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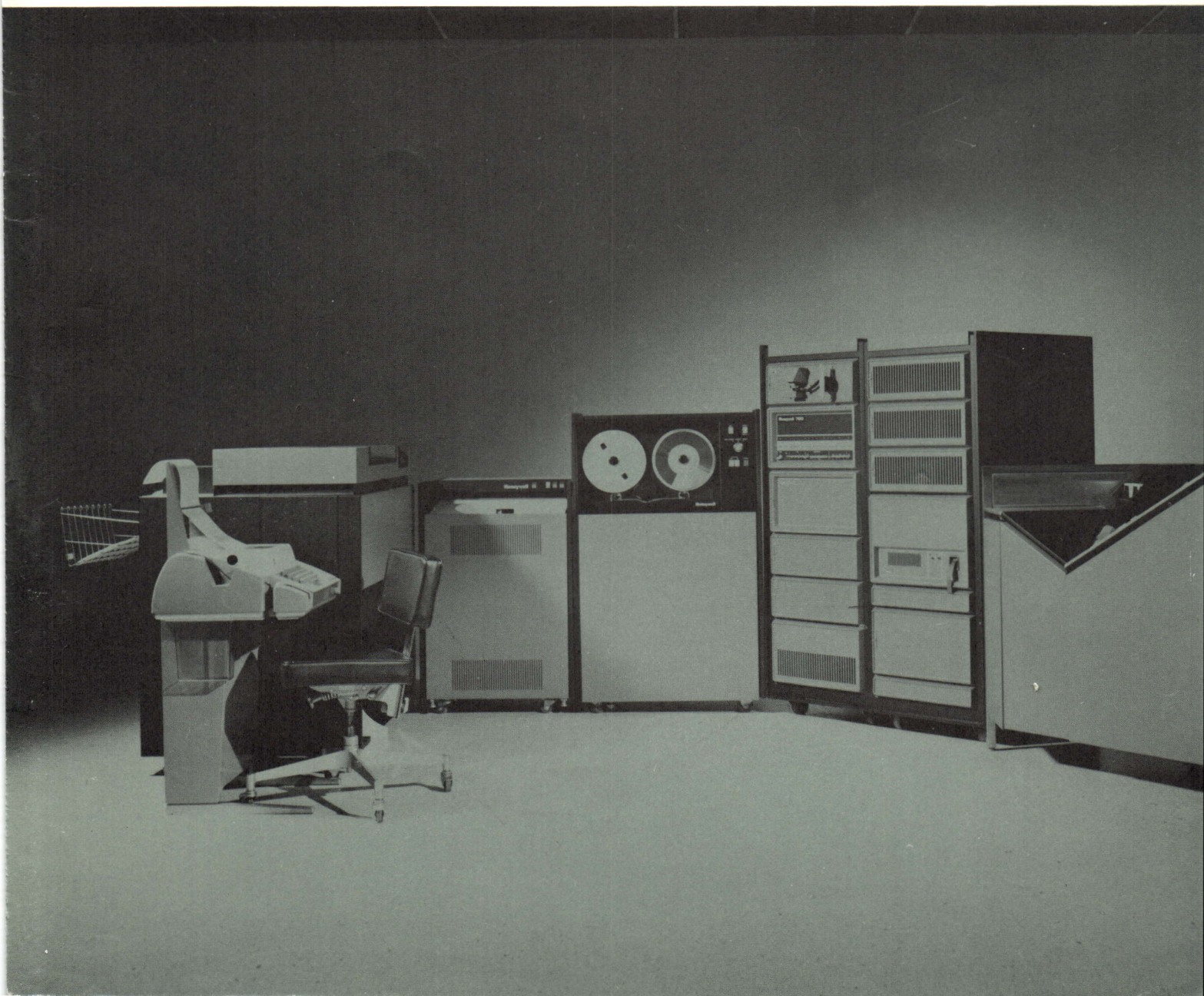
Honeywell

SYSTEM 700

SUMMARY DESCRIPTION



SYSTEM 700

SUMMARY DESCRIPTION

PREFACE

The *System 700 Summary Description* introduces a new series of minicomputer systems. In response to user requests, each system is a hardware/software/support package corresponding to recognized application requirements. Specifications and system features are highlighted in terms that aid comparisons between System 700[1], present processing methods, and competitive proposals. In order that design improvements may be incorporated, the specifications mentioned herein are subject to revision.

[1] Trademark.

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SYSTEM 700: IN RESPONSE TO COMPUTER-USER REQUESTS...

Is it too much to expect a computer company to anticipate the applications of a new line of minicomputers? to expect a large company to respond like a small one? to offer you the specific hardware/software package best suited to your needs? The Other Computer Company doesn't think so. That's why Honeywell offers the applications-oriented System 700 — with a wide spectrum of user-requested capabilities. To name a few:

- Sensor-based systems for manufacturing automation.
- Remote message concentrators for communication control and reduced telephone line costs.
- Terminal and peripheral control systems for factory data collection, material movement, labor reporting, and vehicle scheduling.
- Packaged, preprogrammed, ready-to-run systems.
- Modular systems that offer a choice of cost-effective processing alternatives.
- Features for unattended operation.
- Built-in reliability and data communications capabilities.
- A wide choice of peripheral equipment.
- And a comprehensive library of software.

Just as important as the hardware and software, Honeywell supports System 700 with its worldwide resources — a full spectrum of computer services: business/industry/scientific/government services, education, complete documentation, maintenance services, and systems design.

SIX NEW MINICOMPUTER SYSTEMS

System 700 includes six new models, each based on the Type 716 Central Processor. The processor has an expandable 775-nanosecond main memory and can use single bits of its standard 16-bit words to perform sensing and control functions. The basic central processor has a repertoire of 78 standard instructions, plus versatile addressing techniques, a 16.6 millisecond real-time clock, a control panel, and many other features.

Remote Concentrators — The Model 72050, a general-purpose line concentrator available with optional fast-access disk equipment; and the Model 73050, a factory-configured, ready-to-run remote message concentrator. Both systems contain a 2K-word, nonvolative read-only memory (ROM)[1] to facilitate unattended operation and permit down-line loading from a host computer. Main memory sizes are expandable to 32K words.

Sensor-Based Systems — The Model 72020, a basic configuration that offers limited field expansion, memory sizes up to 16K, and a choice of peripherals; and the Model 72021, a fully expandable configuration, with memory sizes up to 32K and a wider choice of peripherals, including disk.

Terminal and Peripheral Control Systems — Two models that can begin to function at once with a small number of terminals and/or peripherals, while leaving plenty of room for expansion. Model 72001, a terminal-oriented system has an 8K memory expandable to 16K, extensive communication options, but a limited choice of peripherals. Model 72002, a terminal- and peripheral-oriented system, starts with a 16K memory expandable to 32K and offers a wide choice of peripherals and communication options.

SYSTEM 700 HAS RELIABILITY AND DATA COMMUNICATIONS BUILT IN

For many applications, the systems will frequently operate unattended . . . and particularly for remote unattended systems, reliability is an obvious requirement. This is where System 700 excels. The hardware is unquestionably reliable, and of course *designed by the same people who designed the industry's first 16-bit minicomputer.*

Heat dissipation in the central processor is so low that closely regulated air-conditioned environments are unnecessary. The extensive use of integrated circuits and a compact design minimize the number of circuit boards; maintenance, when required, is simple and speedy. For maintenance support, Honeywell offers the worldwide resources of its experienced field engineers, who are as close to you as the nearest telephone.

Standard equipment with System 700 includes power failure detection and automatic restart. If a power failure occurs, the system ensures "graceful degradation" and continuity of operations, and it may perform automatic remote-system recovery . . . all without operator intervention at a remote site. If System 700 is linked to a host sys-

[1] Standard on remote concentrators, optional on other models. ROM stores its information in integrated circuits; programmed at the factory, it never needs to be reloaded.

tem, it can notify the host of the failure, and when power returns, ROM allows the host to down-line load operational software for restoration of the original operating environment.

For protection of the system from illegal program loops, a watchdog timer is offered as standard equipment on the sensor-based systems and remote concentrators and is optional for the terminal and peripheral systems. It can report software faults by "trapping" to the ROM when a loop occurs. The host system can then be informed of the error and can reload operational software or perform diagnostics on line.

To ensure the accuracy of data in a communication network, all incoming data can be checked for validity and accuracy according to terminal-specific tables stored in memory . . . *only completely validated messages are sent on to the host.*

In System 700, data communication is built into the hardware and software. The systems permit the addition of a large number and variety of terminals to a hierarchical system without impact on the host system software.

In addition, a host-resident assembler lets you develop your own software on the host system, where a larger memory and a variety of data processing peripherals are available. After assembly, the new programs can be transmitted down-line to the remote System 700. This way you can keep your remote hardware costs to a minimum without sacrificing the flexibility of a large system.

And . . . instead of visiting each remote system and loading a paper tape when software changes are needed (for example to change a class of line service), you can use ROM to let the host computer down-line load the new software into the remote system. *Software can be updated in minutes instead of days.*

SYSTEM 700 SOFTWARE . . . A PLENTIFUL SUPPLY

Sophisticated software – including the OS/700 Operating System and its powerful programming languages – will give you the kind of control that reduces operator intervention, increases system efficiency, and ensures maximum utilization of the hardware. Among the software components that will support System 700 are:

OS/700 – including a modular, flexible, high-speed, real-time executive. Software will support all available options. Memory required for buffer areas is minimized through the use of dynamic core allocation. The OS/700 executive components will allow users to schedule programs, handle interrupts, coordinate devices, and debug programs.

Fortran IV – a general-purpose, higher level programming language resembling the symbolic language of mathematics . . . designed for more sophisticated problem solving or for the preparation and debugging of programs to be run in the batch environment. It conforms to ANSI Fortran standards and is substantially the same Fortran language as that available on large computers.

BASIC – a stand-alone interpreter that utilizes simple algebraic notation. It is easily learned and well adapted to the concise expression of a wide variety of numerical problems.

DAP/700 – a macro assembler that provides numerous pseudo-operations such as programmer-defined assembly and loader controls, data definitions, and program linkages.

Source Text Editor – a programming aid for updating and correcting DAP/700 and Fortran source code.

Linkage Editor – a single-pass processor that combines various program segments produced by the assembler into a single core image for loading into System 700.

Test and Maintenance Routines – a set of programs for verifying the operation of the control unit, core memory, the arithmetic unit, and the available I/O devices.

2

THE SYSTEMS

TERMINAL AND PERIPHERAL SYSTEMS: FOR DATA COLLECTION AND PROCESSING

The Model 72001 Terminal System and the Model 72002 Peripheral System are versatile members of System 700, well suited to applications requiring data collection via terminals, interactive terminal/computer communications, and data processing. Some of their application areas are:

- Terminal-based factory data collection
- Material movement and labor reporting
- Data entry from medical laboratory terminals
- Data entry from banking terminals

The Terminal System has an 8K-word (16K-byte) memory expandable to 16K words and is available with a basic choice of peripherals and basic data processing capabilities. It can be operated as a limited stand-alone processing system, used to communicate with a host via a single-line controller, or used to collect data via magnetic tape for later processing on the larger host system. The real-time executive of the OS/700 operating system will support the Terminal System. Programming is performed at the assembly language level, with program preparation either on the System 700 or on a host computer by means of the Host-Resident Software System.

The Peripheral System can do everything the Terminal System can – and more. It starts with a 16K-word (32K-byte) memory expandable to 32K words and offer a wide choice of peripherals; it has extensive data processing capabilities. Although primarily a stand-alone system, it may be linked to a larger host system via a communication line controller, or used to collect data via magnetic tape for later processing on the host system. The Peripheral System will make full use of the capabilities of the OS/700 Operating System, including all its language processors – from ANSI Fortran IV to BASIC.

Communication Capabilities

Communication capabilities for the Models 72001 and 72002 are available through the use of a maximum of either two synchronous single-line controllers or a multi function multiline controller. The multiline controller can accommodate up to 16 synchronous and/or asynchronous lines. These models can communicate with other System 700 models, with Honeywell Series 200/2000/600/6000, with IBM 360/370 systems, and others.

Optional communication equipment is listed below.

Type	*Description*
6312	Synchronous Single-Line Controller
6313	Code Convention Option for 6312
6333	Multifunction Multiline Controller (for up to 16 synchronous or asynchronous lines)
6362	Asynchronous Line Unit for 6333 (two lines)
6363	Synchronous Line Unit for 6333 (two lines)

A Choice of Peripherals and Terminals

Models 72001 and 72002 provide facilities for attachment of up to eight console teletypewriters, a paper tape reader and punch, 7- or 9-track magnetic tape units (up to two units for the Model 72001; up to four for the 72002), and communication line controllers. Additional peripheral equipment available for the 72002 includes a card reader or a card reader/punch, a line printer, and one fixed-head disk subsystem (up to one million words of storage) or one removable disk subsystem (up to 15 million words of storage).

The terminals available are ASR-33, ASR-35, and KSR-33 teletypewriters offered by Honeywell; terminals connectable to the single-line controllers, such as Honeywell's 391/392 series; and custom-made terminals using specially designed interfaces.

System 700 peripherals are listed below.

Type	*Description*
For both models	
4021	Magnetic Tape Subsystem (7-track)
4022	Additional Magnetic Tape Unit for 4021
4150	Magnetic Tape Subsystem (9-track)
4153	Additional Magnetic Tape Unit for 4150
5050	Paper Tape Reader and Control
5260	Paper Tape Punch and Control
5307	ASR-33 Teletypewriter
5310	KSR-33 Teletypewriter
5507	ASR-35 Teletypewriter

Type	*Description*
For Model 720/02 only	
5520	Line Printer and Control
5511	Extension of Print Positions (120 to 132)
5121	Card Reader and Control
5140	Card Reader/Punch and Control
4510	Fixed-Head Disk Subsystem (64K words)
4511	Fixed-Head Disk Subsystem (128K words)
4512	Fixed-Head Disk Subsystem (256K words)
4513	Fixed-Head Disk Subsystem (512K words)
4514	Disk Storage Unit (additional 512K words for 4513)
4516	Inert Gas Protection for Fixed-Head Disk Subsystems
4720	Removable Disk Subsystem (7.5 million words)
4721	Additional Disk Pack Drive for 4720

Optional Central Processor Features

To meet individual user requirements, the basic Type 716 Central Processor included with the Terminal System and the Peripheral System can be expanded through optional features. Type 1201 Additional 4K-Word Memory Modules can be added; the maximum capacity of the 72001 is 16K words, and the 72002 can be expanded to 32K words. Feature 1202 provides parity for the first 4K words of memory; Feature 1203 provides parity for each additional 4K words.

Additional equipment available includes Type 1223, 2K Words of Read-Only Memory[1] for the down-line load procedure or any other desired use; Feature 2010, High-Speed Arithmetic Package; Type 3000 Real-Time Clock/Watchdog Timer; and Type 3010 Data Multiplex Control (DMC) Adapter for compatibility with Model 316 and 516 peripheral devices and controls.

Software for the Terminal and Peripheral Systems

OS/700 – to fully support the functions of the Terminal and Peripheral Systems, provided that minimum hardware requirements are met.

Host-Resident Software – a package consisting of the DAP/700 assembler, linkage editor, and configurator, all written in ANSI Fortran IV. Programs may be assembled on a host computer and loaded down-line to the Terminal or Peripheral System.

Test and Maintenance Routines – supplied for the central processor and each of the peripheral devices. These routines are designed to verify the proper operation of the system hardware components and facilitate any required maintenance adjustments.

[1]The user must supply the program to be coded into the ROM.

REMOTE CONCENTRATORS: MINI-MIZE LINE LEASE COSTS AND OFF-LOAD THE HOST

As the number of terminals and long-distance lines in a data communication system increase, line rental becomes a significant part of the total operating cost. System 700 Remote Concentrators can help reduce those costs by concentrating a large number of asynchronous low-speed lines onto one or more synchronous medium-speed lines ... . by concentrating characters originating from remote terminals into complete messages for transmission to the host computer system. Telephone line costs drop sharply.

If the host computer's native code is different from the terminal codes, code conversion must be performed some point in the system. The System 700 Remote Concentrator

RTI EQUIPMENT LIST

RTI equipment available for the sensor-based systems is listed in Table 2.

TABLE 2. RTI EQUIPMENT LIST

Type	*Description*
8515	Subsystem A Controller
8516	Subsystem B Controller
8580	Customer Connection Assembly (Digital I/O)
8581	Customer Connection Assembly (Analog Inputs)
8617	Analog Master Page
8618	Analog Slave Page
8712	Digital I/O Page
8721	Power Supply (24V, 6A) for digital outputs
8722	Power Supply (48V, 3A) for digital outputs
Analog Input Modules	
8631	Low-Level Relay Multiplexer
8634	Open-Thermocouple Detection
8641	High-Level Solid-State Multiplexer (differential input)
8642	High-Level Solid-State Multiplexer (differential input with additional filtering)
8645	High-Level Solid-State Multiplexer (single-ended input)
8653	Amplifier Module (100 mV)
8657	Amplifier Module (10V)
8662	I/V Network (20 mA, 5V)
8664	I/V Network (50 mA, 5V)
8672	RTD Bridge Network (nickel)
8673	RTD Bridge Network (platinum)
8674	RTD Power Supply (w/brackets)
8675	RTD Power Supply
8676	Isothermal Reference Function Unit
8744	Sample and Hold Module
Digital Input Modules	
8731	Status Input Module (contact)
8732	Status Input Module (+6V)
8733	Status Input Module (+24V)
Digital Input Modules (Cont.)	
8741	Asynchronous Input Module (contact)
8742	Asynchronous Input Module (+6V)
8743	Asynchronous Input Module (+24V)
8761	Counter Input Module (8-bit)
8762	Counter Input Module (16-bit)
8764	Preset Counter Input Module (16-bit)
Analog Output Modules	
8061	Analog Output Module (10-bit, ±10V)
8062	Analog Output Module (12-bit, ±10V)
8063	Analog Output Module (12-bit, 0 to 10V)
Digital Output Modules	
8021	Digital Output Module (logic level)
8022	Digital Output Module (power)
8823	D/A Converter (0 to +10V, 20 mA)
8824	D/A Converter (–10 to +10V, 20 mA)
8825	D/A Converter (0 to 25 mA, 800 Ω)
8826	D/A Converter (0 to 50 mA, 320 Ω)
8831	Power Flip-Flop
8841	Power Single-Shot (10 ms)
8842	Power Single-Shot (50 ms)
8843	Power Single-Shot (100 ms)
8844	Power Single-Shot (1000 ms)
8891	Alarm Typewriter Control
Isolated Digital Input/Output Equipment	
8856	Solid-State Medium-Power Switch (AC outputs)
8857	Solid-State Medium-Power Switch (DC outputs)
8858	Isolated Line Voltage Sensor
8861	Relay Output Module (normally open)
8862	Relay Output Module (normally closed)
Output Typewriters	
8868	Selectric Typewriter
8869	Extended Roller for Selectric Typewriter
8870	Selectric Typewriter Control
8892	Alarm Typewriter (60 Hz)
8894	Alarm Typewriter (50 Hz)

with a maximum capacity of 128 multiplexer points. For the Model 72021 Sensor-Based System, a master page and seven slave pages form one analog subsystem of 1024 multiplexer points. For the Model 72020, a master page and up to three slave pages form one analog subsystem of 512 multiplexer points.

A fully expanded AIS on the 72021 consists of two analog subsystems (an A and a B or two A subsystems), with a maximum total of 2,048 analog input points. Each analog subsystem contains independent power supplies, control and address logic, and an A/D converter (with no time-sharing of components), together with integral cooling.

The basic AIS accepts analog multiplexer options: the low-level relay multiplexer and the solid-state, high-level multiplexer. They are provided in groups of eight channels. Submultiplexing groups of eight minimizes the analog bus and capacitance leakage.

Programmed I/O via the central processor I/O bus is the standard method of initiating A/D conversion and subsequent transfer of the converted value to the central processor.

Standard signal-conditioning options interface directly with the AIS. These include current-to-voltage, T/C isothermal compensation, open-circuit thermocouple detection, and resistance-temperature devices.

DIGITAL I/O SUBSYSTEM (DIOS)

The self-contained DIOS (see Figure 4) enables the central processor to accept/transfer digital data to and from external devices. Up to 16 digital I/O options can be accommodated in each master digital page. Expansion to 256 I/O options can be provided by additional pages. Options provide from one to 16 I/O points; e.g., the D/A converter option provides one output point, whereas the status input option accommodates 16.

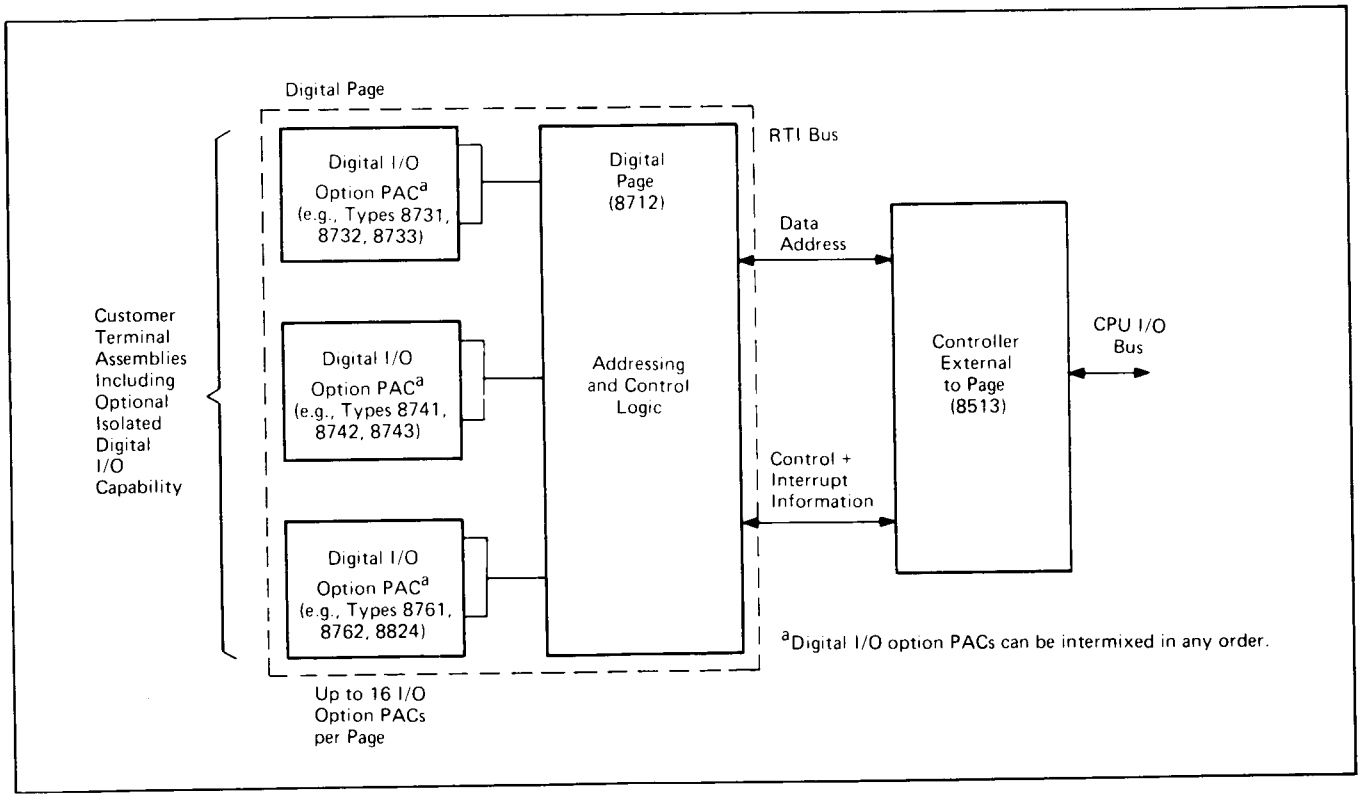


Figure 4. Block Diagram of Digital I/O Subsystem

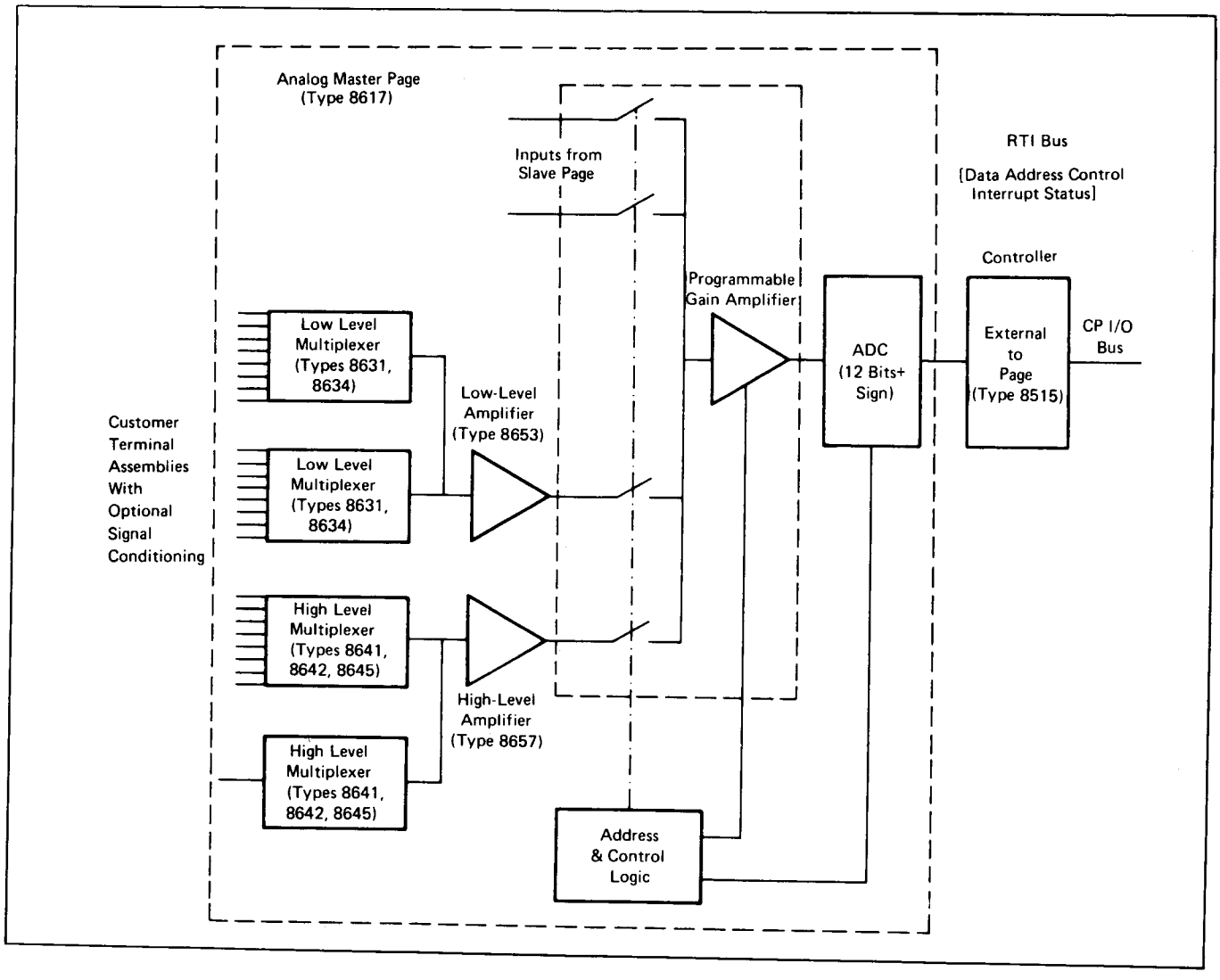


Figure 3. Block Diagram of Analog Input Subsystem

REAL-TIME INTERFACE CONTROLLERS

The Type 8515 Subsystem A Controller and the Type 8516 Subsystem B Controller provide the necessary interface between the real-time interface and the computer. All communications between the RTI and the central processor are accomplished by means of a controller. The central processor services the RTI controllers as if they were peripheral device controls. The Type 8515 operates via the I/O bus and the Type 8516 operates through the DMA.

One subsystem controller is required per RTI subsystem. One Subsystem A Controller is included with the Model 72021; a fully expanded 72021 can accommodate two A controllers and one B controller (up to eight analog and eight digital pages per controller). One controller is included with the Model 72020; the user may select either A or B. The maximum capacity of the Model 72020 is shown in Table 1.

TABLE 1. ANALOG AND DIGITAL PAGE CONFIGURATIONS AVAILABLE FOR MODEL 72020

Digital Pages	Analog Pages	Digital Modules (Max.)	Digital Points	Analog Modules (Max.)	Analog Points
4	—	64	1,024	—	—
3	1	48	768	16	128
2	2	22	512	32	256
1	3	16	256	48	384
—	4	—	—	64	512

ANALOG INPUT SUBSYSTEM (AIS)

The self-contained AIS (see Figure 3), which has only input capability, converts analog information into digital form suitable for the computer. It is subdivided into pages, each

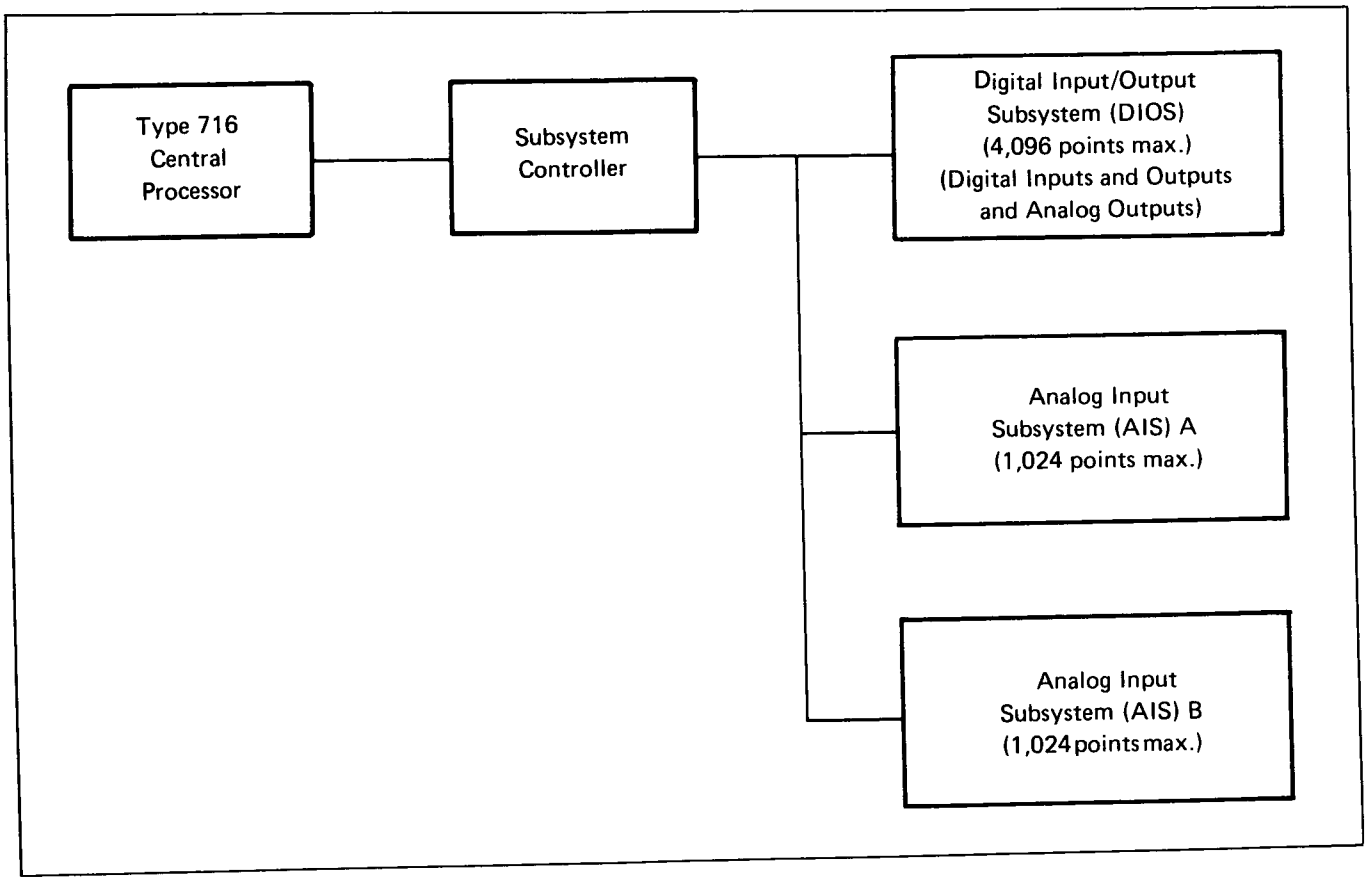


Figure 2. Basic Analog and Digital Subsystem Organization

FUNCTIONS

The Real-Time Interface performs the following functions:

- Decodes input and output instructions from the computer and connects the selected user input or output signals for data transfer.
- Conditions input signals.
- Converts analog input signals into digital form.
- Converts digital data into analog output form.
- Converts signals from computer levels into voltages and currents that can be readily used.
- Protects the computer and related equipment from high-voltage faults.
- Filters noise.
- Provides an easy way to increase the number or change the type of inputs and outputs as the application changes in scope.

FEATURES

Modularity – Incrementally expandable from 8 to 4,096 digital inputs, and from 8 to 2,048 analog inputs, depending on specific configuration requirements.

Field Expandability – Each field expansion of digital and analog input and output signal lines, from smallest to largest.

Versatility – A wide variety of analog signal levels and scanning speeds can be selected. Options include either programmed inputs of single analog values or block transfers. Digital signals can be status inputs (contact), counter inputs, synchronous inputs, flip-flop outputs, pulse outputs, and digital-to-analog converter outputs.

Signal Conditioning – Some of the standard conditioning modules offered are thermocouple isothermal units, current-to-voltage networks, voltage attenuators, and RTD bridges.

Analog Scanning Speed – Up to 125 random input points per second with relay multiplexing and up to 20,000 input points per second with high-level solid-state multiplexing.

Self-Checking – All analog input signals are checked via standard voltages; an open-thermocouple detection circuit is optional.

The second cabinet will hold up to four analog and digital pages in any combination.

Also included with the Models 72020 and 72021 is a real-time clock/watchdog timer to facilitate unattended operation and protect the system from illegal program loops.

Communication Capabilities

Although the Models 72020 and 72021 are primarily stand-alone systems, communications capabilities are available through the use of a Type 6333 Multifunction Line Controller (MFMLC). The MFMLC can accommodate up to 16 lines by the use of Type 6362 Asynchronous and Type 6363 Synchronous Line Units. The systems can communicate with other System 700 configurations, Honeywell Series 200/2000/600/6000, IBM 360/370 systems, and others.

Software

OS/700 – this real-time operating system will fully support the functions of the sensor-based systems, provided that the minimum hardware requirements are met.

Host-Resident Software – a package consisting of the System 700 macro assembler, linkage editor, and configurator, all written in ANSI Fortran IV. Programs may be assembled on a host computer and loaded down-line to the Model 72020 or 72021.

Peripherals

Peripherals available with the 72021 system include a maximum of one million words of fixed-head disk storage, up to two 7- or 9-track magnetic tape units, a paper tape reader and a paper tape punch, and up to six teletypewriters. Peripherals available with the 72020 are up to two 7- or 9-track magnetic tape units, a paper tape reader and a paper tape punch, and up to six teletypewriters. Optional peripherals for sensor-based systems are listed below.

Type	*Description*
4021	Magnetic Tape Subsystem (7-track)
4022	Additional Magnetic Tape Unit for 4021
4150	Magnetic Tape Subsystem (9-track)
4153	Magnetic Tape Unit for 4150
4510[1]	Fixed-Head Disk Subsystem (64K words)
4511[1]	Fixed-Head Disk Subsystem (128K words)
4512[1]	Fixed-Head Disk Subsystem (256K words)
4513[1]	Fixed-Head Disk Subsystem (512K words)
4514[1]	Disk Storage Unit (additional 512K-word capacity for the Type 4513)
4516[1]	Inert Gas for Fixed-Head Disk Subsystem
5050	Paper Tape Reader and Control
5260	Paper Tape Punch and Control
5307	ASR-33 Teletypewriter and Control
5310	KSR-33 Teletypewriter and Control
5507	ASR-35 Teletypewriter and Control

[1] Available only on the Model 72021.

Optional Central Processor Equipment

In addition to the wide selection of real-time interface equipment (described below) and data processing peripheral equipment, the following optional equipment is available for the central processor in Model 72020 and 72021 systems.

Type	*Description*
1201	4K Words (8K bytes) of Main Memory
1202	Parity for First 4K Words of Main Memory
1203	Parity for Each Additional 4K Words of Main Memory
1223	2K ROM for Customer-Supplied Program
2010	High-Speed Arithmetic and Base Sector Relocation
3010	Data Multiplex Control Adapter

Real-Time Interface (RTI): Analog and Digital Input/Output Subsystems

The RTI is the result of over ten years' experience in real-time control systems. It provides a flexible, reliable interface between the control computer and a diversity of sensors, field contacts, logic signals, control elements, and many other devices. The RTI provides multiplexing, isolation, and signal conditioning. The wide array of input and output equipment includes thermocouple isothermal units, current-to-voltage networks, high- and low-level analog input modules, and a variety of digital input and output modules.

This equipment is mounted in the analog and digital subsystems. (Figure 2 shows the basic analog and digital subsystem organization.) Each subsystem in turn is made up of pages, which are vertical swing-out drawers, capable of holding 16 option PACs (modules) each. Each page contains all necessary logic power supplies, control logic, and connector slots. The number of digital input/outputs on each module varies with the function; however, a digital page can accommodate up to 256 input/outputs and an analog page can accommodate up to 128 inputs.

the Host-Resident Software System. A package consisting of the DAP/700 assembler, linkage editor, and configurator – the Host-Resident Software will provide for assembly, linkage editing, and reconfiguring on the host.

CONSIDER THE SENSOR-BASED SYSTEMS . . . WHATEVER THE LINK OR THE MEASUREMENT

Whatever has to be measured – analog or digital – chances are you'll find a System 700 Sensor-Based System to match the application. As an "intelligent" feedback system to replace inflexible analog or digital control devices . . . as a means of decentralizing a large central control system . . . as an unbeatable hardware/software/support package to reduce manpower requirements and improve operation discipline . . . a Sensor-Based System offers capabilities for

- Industrial and medical laboratory reporting
- Material movement and labor reporting
- Process control
- Factory data collection
- Testing
- Data logging and reduction
- Warehousing
- And any other application where a measurement is required

System 700 becomes a key element in your business when you tie it into your present data processing system – a Honeywell 200/2000/600/6000, an IBM 360/370, or other large systems using binary synchronous communications. Whether the sensor-based system is linked directly, remotely, or manually to the central processors, the resulting economies soon justify the change in method, even if your method is already computer-controlled.

The functions of a sensor-based system can vary from the simple recording of a few data measurement devices to the multisystem, multifunction, hierarchical use of System 700 to acquire data, test its status against an established norm, branch to routines that direct further action, and communicate some results to a larger host system. With the sensor-based systems, applications are limited only by the number of procedures that exist in an industrial or scientific operation, and the costs are comparable with those of any present method.

A sensor-based system includes a central processor and an input/output subsystem interfacing both men and machines. Those devices interfacing people in a typical application include control consoles, paper tape readers and punches, magnetic tape subsystems, and fixed-head disk subsystems. From this array, you can choose the mix of input, output, and bulk storage that suits your needs.

To control real-time procedures, you can select the components that interface with your measurement devices. Typical devices for input include thermocouples, RTDs, flowmeters, pressure transducers, and tachometers; for output: lights, relays, starters, valves, control stations, and set points.

The Model 72020 Sensor-Based System is a basic configuration that offers limited field expansion and a choice of peripherals. It includes a Type 716 Central Processor with an 8K-word memory (expandable to 16K), a real-time interface controller, and two 72-inch cabinets with power distribution units. The system can accommodate a total of four pages (analog, digital, or both) for controlling input/output modules.

The Model 72021 Sensor-Based System is a fully expandable configuration with a wider choice of peripherals. It includes a Type 716 Central Processor with a 16K-word memory (expandable to 32K), a real-time interface controller, a digital page, and two 72-inch cabinets with power distribution units. The cabinet housing the central processor can accommodate expansion drawers, as well as peripherals such as the fixed-head disk and paper tape reader and punch.

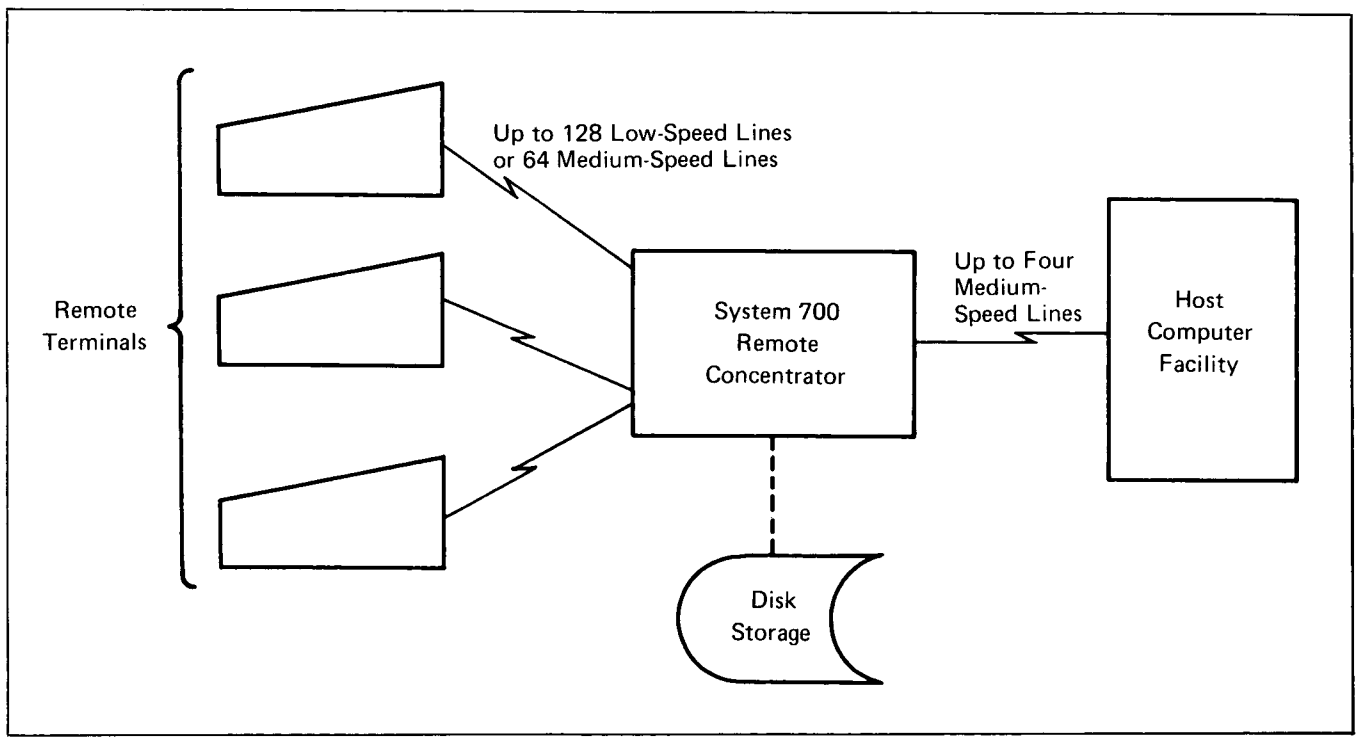


Figure 1. System 700 for Remote Line and Message Concentration

Remote Line Concentrator is custom tailored

In addition to basic message concentration, the Model 72050 Remote Line Concentrator offers extended communication capabilities that can be used for editing and the addition of information (e.g., time of day) to each message. Virtually any computing system requiring multiple terminals and special concentrator activity can successfully use the Model 72050.

This model consists of a Type 716 Central Processor with 8K words of memory expandable to 32K, a 2K ROM programmed at the factory according to customer design specifications, a real-time clock/watchdog timer, a synchronous single-line controller, a low-speed or universal multiline controller, and the necessary cabinetry. Memory can be added to accommodate lines and user-supplied functions, the amount depending on the number of lines and the extent of user programs. Up to one million words of fixed-head disk storage is optional. An ASR-33 or -35 or a KSR-33 teletypewriter is required.

Options available on the Model 72050 include the following:

Type	*Description*
4510	Fixed-Head Disk Subsystem (64K words)
4511	Fixed-Head Disk Subsystem (128K words)
4512	Fixed-Head Disk Subsystem (256K words)
4513	Fixed-Head Disk Subsystem (512K words)
4514	Disk Storage Unit (additional 512K-word capacity for the Type 4513)
4516	Inert Gas for Fixed-Head Disk Subsystem
5307	ASR-33 Teletypewriter and Control
5310	KSR-33 Teletypewriter and Control
5507	ASR-35 Teletypewriter and Control
6312	Synchronous Single-Line Controller
6313	Code Convention Option
6333	Multifunction Multiline Controller
6362	Asynchronous Line Unit for 6333 (2 lines)
6363	Synchronous Line Unit for 6333 (2 lines)

Software that will support the Model 72050 includes the real-time executive of the OS/700 Operating System and

can perform code conversion, polling, adaptive line speed control, error detection and correction. The result: the host computer is relieved from directly handling a whole network of separate lines at separate speeds for separate terminals, and from performing time- and core-consuming message processing functions. With all code conversion performed by System 700, data flowing in each direction is in the host's native code.

The work that can be off-loaded from the host can make the difference between a well-balanced host processing load and an overloaded system (which would otherwise require a costly upgrade or degraded service to revenue-producing or cost-saving main system tasks).

Here are some more advantages of System 700 Remote Concentrators:

- Reduce the number of long-distance lines.
- Justify the cost of convenient leased lines for improved service.
- Provide higher concentration ratios and greater flexibility than available with hard-wired multiplexers.
- Offer software-selectable line speeds.
- Permit multiple-speed terminals to operate on the same line.
- Provide communication with other System 700 models, with Honeywell Series 200/2000/600/6000, with IBM 360/370, and with others.
- Use medium-bandwidth lines efficiently.
- Buffer messages.
- Provide cyclic redundancy checks (CRC) and full hardware control of BSC lines.
- Detect power failures and restart automatically.
- Down-line load operational software via ROM.

Standard, off-the-shelf concentrator is ready to run

The Model 73050 Remote Message Concentrator consists of a configured combination of hardware and software elements to concentrate up to 128 full-duplex lines at 300 baud, or up to 64 full-duplex lines at 2400 baud, onto an appropriate medium-speed line to a host computer (see Figure 1).

The basic version of the model consists of a Type 716 Central Processor with 12K words of memory expandable to 32K; a 2K loader in ROM; a real-time clock/watchdog timer: a synchronous single-line controller; a low-speed or universal multiline controller; and the required cabinetry. The basic system will support up to 16 lines. Memory must be added to accommodate extra lines, as follows:

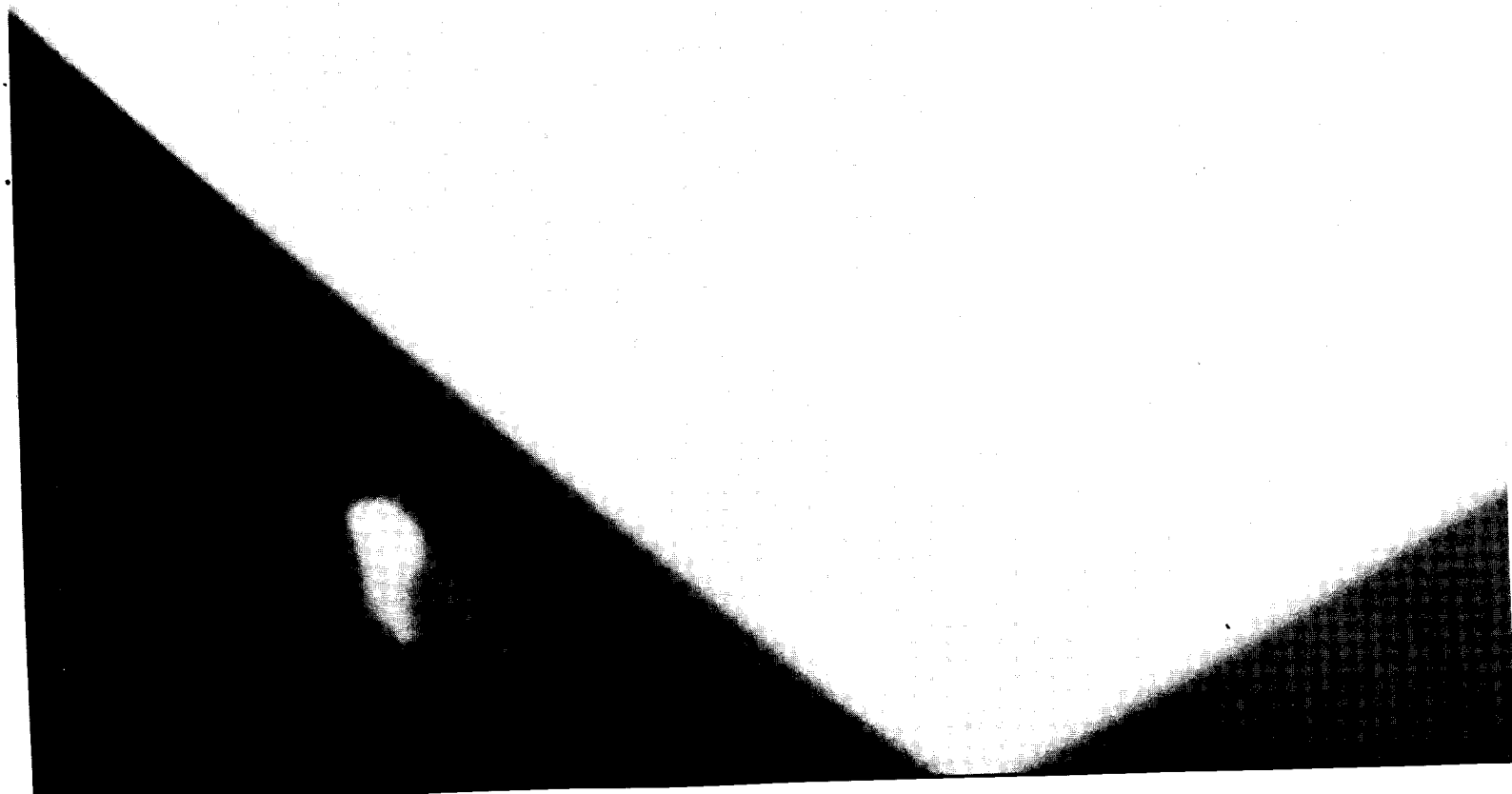
Lines	*Additional Memory (words)*
16-39	16K
40-63	20K
64-95	24K
96-127	28K
128	32K

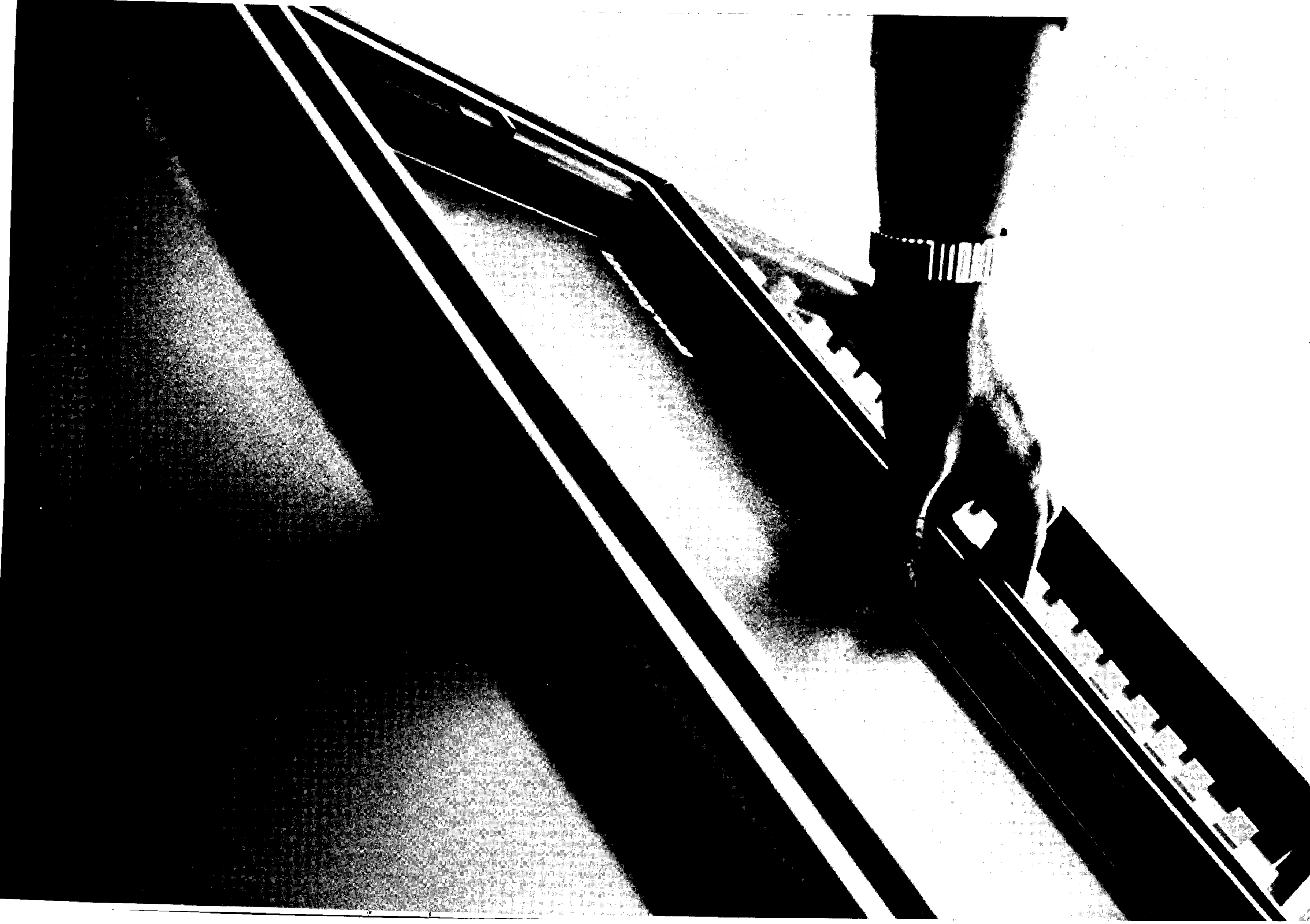
An ASR-33 or -35 or a KSR-33 teletypewriter is required.

Options available on the Model 730/50:

Type	*Description*
1201	4K Words (8K bytes) of Main Memory
1201	Parity for First 4K Words of Main Memory
1203	Parity for Additional 4K Words of Main Memory
5307	ASR-33 Teletypewriter and Control
5310	KSR-33 Teletypewriter and Control
5507	ASR-35 Teletypewriter and Control
6312	Synchronous Single-Line Controller
6313	Code Convention Option
6321	Low-Speed Multiline Controller
6322	Universal Multiline Controller
6333	Medium-Speed Multiline Controller
6362	Asynchronous Line Adapter for 6333 (2 lines)
6363	Synchronous Line Adapter for 6333 (2 lines)
6351	103 Line Module (4 lines)
6352	Asynchronous Line Module (2 lines)
6353	Synchronous Line Module (2 lines)
6925	Synchronous Modem Bypass
6926	Asynchronous Modem Bypass

The Model 73050 is delivered with a completely configured software system. However, if expansion is desired, a Host-Resident Software System – including an assembler, linkage editor, and configurator – all written in ANSI Fortran IV, will provide for reconfiguring on the host. Programs can then be loaded down-line. Also available are a library of host control processors (HCP) and terminal control processors (TCP), so that many types of terminals may be added without impact on the System 700 software.





3

FOR SENSING, COMMUNICATION, CONTROL... THE 716 CENTRAL PROCESSOR

In each of the System 700 minicomputer systems, the common denominator is the basic Type 716 Central Processor – a 16-bit-word, high-performance minicomputer. With its 775-nanoseconds-per-word cycle time and high I/O throughput facilities, the user is assured maximum system utilization. The 716 is a solid-state digital processor organized on a single-address, TWOs complement basis.

Its standard features include:

- Control panel for displaying and controlling registers and states in the processor.
- Keylock for control panel to prevent unauthorized use.
- Operator's halt register to facilitate debugging.
- 20 ms real-time clock.
- Power failure interrupt.
- Automatic restart after power failure.
- Trace interrupt to facilitate program debugging.
- Stack overflow/underflow interrupt.

The processor has a repertoire of 78 standard instructions, consisting of the Honeywell Series 16 instruction set plus added instructions and addressing techniques. With the standard instruction set and high-speed memory, the Type 716 can effectively handle data minipulation, control, arithmetic, byte-processing, and input/output operations. Its standard processing capabilities and instruction set can be expanded by optional features:

- *High-Speed Arithmetic Package* – includes hardware multiply/divide and floating-point operations, a virtual necessity for applications requiring control equations and extensive problem-solving capabilities.
- *Main Memory Parity* – provides parity checking and additional instructions.
- *Real-Time Clock and Watchdog Timer* – for protection of the system from illegal program loops; includes additional instructions and two timers that can be used together or independently.
- *Data Multiplex Control Adapter* – for compatibility with Series 16 peripheral devices and controls.
- *Read-Only Memory (ROM)* – for nonvolatile storage of programs; never needs reloading; facilitates unattended operation and down-line loading.
- Additional main memory in 4K-word increments.

Memory and input/output options can be intermixed on the processor's I/O bus. The I/O bus is implemented as a printed-circuit backplane with signals for both the memory and I/O options.

The central processor is housed in a rack-mountable drawer which is approximately 267 mm high by 432 mm wide by 559 mm deep and can be mounted in a standard, 483 mm wide cabinet. The circuits are packaged on eleven 252 mm by 259 mm boards. Eight additional card slots are available in the processor drawer for either device control units or memory. Additional card slots are also available in expansion drawers.

The Type 716 Central Processor comprises three major components:

- The processing unit,
- The input/output system, and
- Main memory and read-only memory.

THE PROCESSING UNIT

The processing unit is the computing and control center of the Type 716 Central Processor. Design features include:

- An extensive instruction set (see Table 3), with many instructions requiring only one memory cycle for execution.
- Simple, easy-to-understand operation procedures.
- Built-in power failure protection and auto restart.
- Real-time clock (20 ms)

In the processing unit are the registers that store, compute, and transfer data under program control. The major registers available to the programmer include two arithmetic registers, one program counter, and two index registers – one of which can be used as a hardware stack register.

TABLE 3. INSTRUCTION REPERTOIRE WITH EXECUTION TIMINGS

OP Code	Mnemonic	Description	Type	Execution Time (ns)	Notes
01	JMP,JMPQ	Unconditional Jump	MR	775	1
02	LDA,LDAQ	Load A-Register	MR	1550	1
02	DLD,DLDQ	Double-Precision Load	MR	2325	1,2,3
03	ANA,ANAQ	AND Memory with A-Register	MR	1550	1
04	STA,STAQ	Store A-Register	MR	1550	1
04	DST,DSTQ	Double-Precision Store	MR	2325	1,2,3
05	ERA,ERAQ	EXCLUSIVE OR Memory with A-Register	MR	1550	1
06	ADD,ADDQ	Add	MR	1550	1
06	DAD,DADQ	Double-Precision Add	MR	2325	1,2,3
07	SUB,SUBQ	Subtract	MR	1550	1
07	DSB,DSBQ	Double-Precision Subtract	MR	2325	1,2,3
10	JST,JSTQ	Jump and Store Location	MR	2325	1
11	CAS,CASQ	Compare	MR	1550+350C	1
12	IRS,IRSQ	Increment, Replace, and Skip	MR	2325	1
13	IMA,IMAQ	Interchange Memory and A-Register	MR	2325	1
14	OCP	Output Control Pulse	I/O	2320	
15	LDX,LDXQ	Load X-Register	MR	2325	1,4
15	STX,STXQ	Store X-Register	MR	1550	1,4
16	MPY,MPYQ	Multiply	MR	3925	1,2
17	DIV,DIVQ	Divide	MR	6975	1,2
34	SKS	Skip on Sense Line	I/O	2300	
54	INA	Input to A-Register	I/O	2300	
74	OTA	Output from A-Register	I/O	2300	5
74	SMK	Set Mask	I/O	2300	5
0400	LRL	Long Logical Right Shift	SH	775+350N	
0401	LRS	Long Arithmetic Right Shift	SH	775+350N	
0402	LRR	Long Right Rotate	SH	775+350N	
0404	LGR	Logical Right Shift	SH	775+350N	
0405	ARS	Arithmetic Right Shift	SH	775+350N	
0406	ARR	Right Rotate	SH	775+350N	
0410	LLL	Long Logical Left Shift	SH	775+350N	
0411	LLS	Long Arithmetic Left Shift	SH	775+350N	
0412	LLR	Long Left Rotate	SH	775+350N	
0414	LGL	Logical Left Shift	SH	775+350N	
0415	ALS	Arithmetic Left Shift	SH	775+350N	
0416	ALR	Left Rotate	SH	775+350N	
000000	HLT	Halt	G	775	
000005	SGL	Enter Single-Precision Mode	G	775	2
000007	DBL	Enter Double-Precision Mode	G	775	2
000011	DXA	Disable Extended Addressing	G	775	
000013	EXA	Enable Extended Addressing	G	775	
000015	XFX	Index from X-Register	G	775	
000017	XFS	Index from S-Register	G	775	
000021	RMP	Reset Memory Parity Error	G	775	2
000041	SCA	Shift Count to A-Register	G	775	2
000043	INK	Input Keys	G	775	
000101	NRM	Normalize	G	775+350N	2

TABLE 3. (Cont.) INSTRUCTION REPERTOIRE WITH EXECUTION TIMINGS

OP Code	Mnemonic	Description	Type	Execution Time (ns)	Notes
000201	IAB	Interchange A- and B-Registers	G	775	
000401	ENB	Enable Interrupts	G	775	
001001	INH	Inhibit Interrupts	G	775	
001401	ERM	Enter Restrict Mode	G	775	2
004005	POP A (LDA 5)	Pop Stack Top to A-Register	SMR	2325	
010004	PUSH A (STA 4)	Push A-Register onto Stack	SMR	2325	
020004	PUSH P (JST 4)	Push P-Register onto Stack	SMR	2325	
024003	POP (IRS 3)	Discard Top Element of Stack	SMR	2325	
032004	PUSH X (STX 4)	Push X-Register onto Stack	SMR	2325	
072005	POP X	Pop Stack Top to X-Register	SMR	3100	
100000	SKP	Unconditional Skip	G	775	
100001	SRC	Skip if 0-Bit = 0	G	775	
100002	SR4	Skip if Switch 4 is Reset	G	775	
100004	SR3	Skip if Switch 3 is Reset	G	775	
100010	SR2	Skip if Switch 2 is Reset	G	775	
100020	SR1	Skip if Switch 1 is Reset	G	775	
100036	SSR	Skip if no Switch is Set	G	775	
100040	SZE	Skip if A-Register Zero	G	775	
100100	SLZ	Skip if A-Register Bit 16 = 0	G	775	
100200	SPN	Skip if no Memory Parity Error	G	775	2
100400	SPL	Skip if A-Register Positive or Zero	G	775	
101000	NOP	No Operation	G	775	
101001	SSC	Skip if C-Bit = 1	G	775	
101002	SS4	Skip if Switch 4 is Set	G	775	
101004	SS3	Skip if Switch 3 is Set	G	775	
101010	SS2	Skip if Switch 2 is Set	G	775	
101020	SS1	Skip if Switch 1 is Set	G	775	
101036	SSS	Skip if Any Switch is Set	G	775	
101040	SNZ	Skip if A-Register not Zero	G	775	
101100	SLN	Skip if A-Register Bit 16 = 1	G	775	
101200	SPS	Skip if Memory Parity Error	G	775	2
101400	SMI	Skip if A-Register Negative	G	775	
102005	POP P (JMP* 5)	Pop Stack Top to P-Register	SMR	2325	
102005	RTN (JMP* 5)	Pop and Return through Stack Top	SMR	2325	
140024	CHS	Complement Sign	G	775	
140040	CRA	Clear A-Register	G	775	
140100	SSP	Set Sign Plus	G	775	
140200	RCB	Reset C-Bit	G	775	
140320	CSA	Copy Sign and Set Sign Plus	G	775	

TABLE 3. (Cont.) INSTRUCTION REPERTOIRE WITH EXECUTION TIMINGS

OP Code	Mnemonic	Description	Type	Execution Time (ns)	Notes
140401	CMA	ONEs Complement A-Register	G	775	
140407	TCA	TWOs Complement A-Register	G	775	
140500	SSM	Set Sign Minus	G	775	
140600	SCB	Set C-Bit	G	775	
141044	CAR	Clear A-Register, Right Half	G	775	
141050	CAL	Clear A-Register, Left Half	G	775	
141140	ICL	Interchange and Clear Left Half of A-Register	G	775	
141206	AOA	Add One to A-Register	G	775	
141216	ACA	Add C-Bit to A-Register	G	775	
141240	ICR	Interchange and Clear Right Half of A-Register	G	775	
141340	ICA	Interchange Characters in A-Register	G	775	
170024	CAI	Clear Active Interrupt	I/O	2300	5
171020	OTK	Output Keys	I/O	2300	5

The mnemonics shown with Q are valid to the OS/700 Macro Assembler only when followed by one of the special names, X, A, B, S, T, W, and I, where X means 0, A means 1, B means 2, S means 3, T (Top) means indirect through 3, I(Insert) means 4, and W (Withdraw) means 5.

Type Abbreviations

MR = Memory Reference
I/O = Input/Output
G = Generic
SMR = Specially Defined Memory Reference
SH = Shift

Execution Time

C = 0 if the contents of the A-register are equal to or greater than the contents of the core location specified by the effective operand address; otherwise C = 1.

N = Number of places shifted minus one for shifts (= number of places shifted for NRM); = 0 for shifts or NRMs of 0 places.

Notes:

1. Instructions utilizing special addresses 4 and 5 (I and W) require an additional 775 ns.
2. Optional instruction.
3. CPU must be in double-precision mode.
4. Instructions STX and LDX have the same operation code (15). STX has an index bit of 0; LDX has an index bit of 1.
5. Instructions OTA, SMK, OTK, and CAI have the same operation code (74). OTA may have any device code, but the others are limited to '20 or '24. OTK and CAI have a dedicated function code as well.

Programs are executed sequentially with the contents of the program counter (P-register) incrementing by one upon the execution of each instruction. Certain instructions (SKIPS, COMPARE, I/O) conditionally increment the program counter by an additional one or two, thereby causing a skip. Others (JUMP, JUMP-STORE) unconditionally load the program counter with a new effective address, thereby causing a branch in the program.

The System 700 processor features a repertoire of instructions which, with tremendous flexibility and power, can handle all arithmetic, logical, control, and input/output functions necessary for control and communication processing. Also included in the processors are instructions dealing with peripherals and communications interrupts and for handling data in 5- to 8-level codes.

Processor Operation

The Type 716 processor is operator-oriented. With the computer operator in mind, Honeywell engineers designed the system to display extensive control information but allowed for flexibility to satisfy user requirements.

The standard control panel on the front of the processor contains binary displays in octal representation, run status displays, and all operator controls. By pressing the appropriate select switch, the operator can display register contents and memory information as well as internal counters and flip-flop status.

Registers can be cleared and/or altered from the panel, and the contents of memory locations can be displayed or changed. (Memory locations 1-17 contain program load instructions and can be loaded manually only.)

Other control panel functions include selection of the operation mode (memory access, single instruction, continuous run), four sense switches for control of programs, and a power failure interrupt inhibit switch. The control panel also provides an operator's halt register to aid program debugging.

In addition to a control panel, a teletypewriter keyboard unit with (or without) a paper tape reader and punch is available for the System 700 Processor. When used in conjunction with software checkout functions, this I/O device becomes the primary control for breakpointing programs, changing memory contents, displaying memory, and related functions. It can also be used off-line for preparation, duplication, or listing of program tapes.

TABLE 4. SUMMARY OF PROCESSING REGISTERS

Register	Function	Mnemonic
	Control Registers	
Program Counter	15-bit register containing the location of the next instruction to be executed.	P
Memory Register	16-bit register used to transfer information to and from memory.	M
Address Register	15-bit register containing the location in memory to or from which information is being transferred.	Y
Index Register	16-bit register used in address modification.	X
Stack or Index Register	16-bit stack-top pointer or alternative index register.	S
	Arithmetic Registers	
Primary Arithmetic Register	16-bit register in which all arithmetic and logical bit manipulation occurs.	A
Secondary Arithmetic Register	16-bit register used in conjunction with A when arithmetic operands exceed one word in length.	B
Overflow or Carry Bit	1-bit register used to indicate an overflow or carry condition.	C
Adder	logic gating, which performs all arithmetic operations.	

Control Registers

There are five processing control registers. These registers (see Table 4) normally contain the addresses of instructions and data being processed during a program run. For example, the address register (Y-register) contains the location in memory to which information is being transferred or from which it is being retrieved. The operation in which the value of this location is established is called "effective address formation." Figure 5 illustrates this typical control unit function. In the illustration, an instruction stored in memory is loaded in the memory register (M-register). After the address portion of this instruction is added to the portion of the program counter (P-register) that designates the memory sector, the result is stored in the Y-register as the instruction is executed.

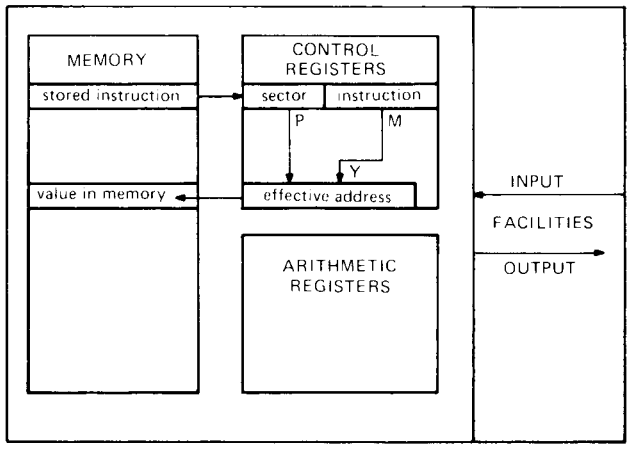


Figure 5. Typical System 700 Control Register Activity

The stack register provides the hardware for reading and writing lists. On the Type 716 Central Processor, this register is a push-pop stack, i.e., it is a last-in/first-out stack. The stack register is used to form message or priority queues. For interruptible software, the stack can be used to store the contents of registers so that the interrupted program can be restored.

On the Type 716 processor control registers can be displayed at the operator's control console. For instance, the operator can interrogate the program counter to determine the exact location at which a program has halted. A register is addressed from the control panel by pressing the appropriate push buttons; the contents will appear in an "on" or "off" status on the 16 control panel indicators that represent a memory location.

The index register (X-register), if indexed addressing is specified, is utilized in address formation and modification.

Arithmetic Registers

Arithmetic and logical operations are performed in the adder and in a series of arithmetic registers (Table 4). Including a primary arithmetic register (A-register), a secondary arithmetic register (B-register), and an overflow indicator (C-bit), the arithmetic registers give the processors the great computing flexibility so important to process and bit manipulation application.

Figure 6 illustrates a typical arithmetic function – an add operation. Before this operation begins, the control registers have established the "effective address" in memory and the nature of the operation to be performed has been stored. Acting under these established facts, the control directs the addition operation. If the programmer desires to return the sum to a location in memory, another instruction is required.

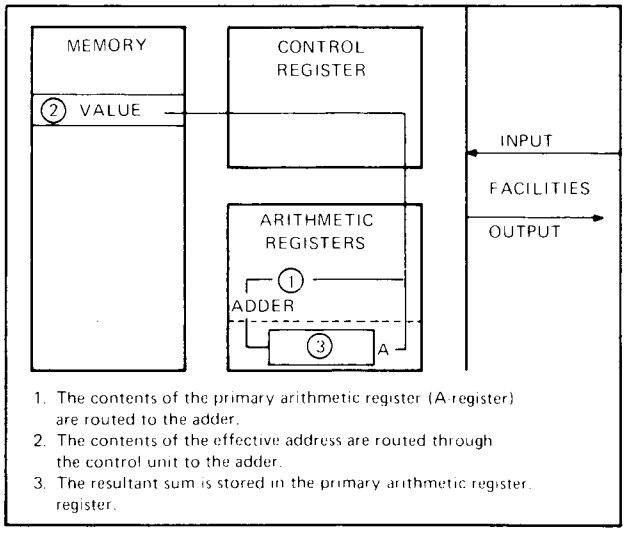


Figure 6. Typical System 700 Arithmetic Function

The functioning of the other arithmetic registers, the B-register and the C-bit, depends on the nature of the instructions being executed.

The arithmetic registers are accessible from the control console as well as by programmed instruction. An operator can change their contents.

Both the control and the arithmetic registers function under the control of a clocking system that enables the processor to rapidly select, interpret, and execute all instructions in a stored program. This clocking system also coordinates the various activities of receiving data from input devices and transferring data to output devices.

INPUT/OUTPUT SYSTEM

The input/output system regulates the flow of data, instructions, and control information between main memory and peripheral device controls. As in most computer systems, it works in conjunction with the system software, main memory, and peripheral controls to allocate central processor time to input/output operations, to identify peripheral controls that will use that time for data transfers, and to use a priority system for accesses to memory.

But unlike many other systems, the 716's I/O system uses a new distributed priority network that takes the burden off the central processor's I/O logic for the control of peripheral data transfers. The controls for the new System 700 peripheral devices now perform many control tasks that would otherwise require central processor time and resources.

An added feature of the new I/O system design is the use of a star configuration, rather than the conventional "daisy chain," for the location of peripheral devices, thus giving added flexibility for the arrangement of the computer room.

The input/output system supports three classes of I/O operations: programmed input/output via instructions, direct memory access, and distributed priority interrupt.

Programmed I/O via Instructions

Functions of programmed I/O are:

- Outputting control information to a device (such as "read a tape record."
- Setting up for a DMA[1] data transfer.
- Transferring data, if the device characteristics allow programmed I/O (e.g., teletypewriters and paper tape equipment).
- Checking the status of a device.

The structure of the I/O system provides a simplified means for checking device status. Using a single program instruction, the programmer can bring 16 bits into memory at a time to check several status conditions (e.g., power on, device ready, device not busy).

Direct Memory Access (DMA)

The DMA provides an alternative path to memory for high-speed data transfers. I/O transfers that use the DMA are processed on a cycle-stealing basis and proceed automatically after a programmed I/O instruction has been issued. Up to 32 peripheral controls, each with its own address and range registers, can be multiplexed into the DMA to allow simultaneous and independent data transfers.

[1] DMC transfer operation is available with the optional Type 3010 DMC Adaptor

Here are some of the advantages of DMA:

- Overlapped operation – while one I/D data transfer takes place, another peripheral control is setting up for a transfer.
- Peripheral control priority determined by a distributed priority network and position on the I/O bus; priority is resolved before data transfer takes place – no wait.
- Fast response to peripheral device requests for access to memory, because DMA has highest priority break request.
- Byte or word transfers.
- Parity checking for DMA transfers on the I/O bus (one parity bit per byte).

Priority Interrupts

A priority interrupt causes a jump from the current program to another program at the end of an instruction execution. The distributed priority network allows the programmer to specify that lower priority interrupts be inhibited without inhibiting higher priority interrupts. Thus, higher priority interrupts can be serviced more quickly. In addition, the normal priority of the distributed priority network can be overridden by the programmer.

The new distributed priority network is particularly efficient in the processing of priority interrupts. It eliminates the need for the programmer to code instructions that cause polling of peripheral devices to determine the source of an interrupt. With the new design, a peripheral control sends to the central processor the address of its controlling program's starting location. Thus, with the peripheral controls handling this identification function, the central processor is free for other activities. Up to 32 peripheral controls can be attached to the distributed priority network; the physical location of the peripheral control on the I/O bus determines the interrupt priority.

MAIN MEMORY

In the Type 716 Central Processor, main memory consists of a memory controller and up to eight 4K-word magnetic-core storage modules. Storage capacities range from 8K to 32K words. The cycle time required to read and restore the contents of a memory location is 775 nanoseconds.

Both program instructions and the data to be manipulated by the program reside in memory during a program operation. As a key to programming, every word is identified by a unique numeric address.

Access to Main Memory

Priority access to memory is important to the real-time power of the System 700 processor. The various functions of the input/output and processing logic are executed in a priority sequence when two or more functions request access to main memory simultaneously. The priorities are:

1. Direct Memory Access
2. Data Multiplex Control Break
3. Real-Time Clock Increment
4. Power Failure Interrupt/Watchdog Timer
5. Trace Interrupt
6. Stack Overflow/Underflow Interrupt
7. 316/516 Compatible Interrupts
8. Standard 716 I/O Bus Interrupts
9. Program Execution

Breaks

Certain operations may occur between instructions without affecting the contents of the program counter. When the operations are complete, the program resumes. These actions are called "breaks" and include the operation of transferring data via DMA or DMC and incrementing the real-time clock.

It may be noted that the program being executed and other operations are always computing and vying for access to memory. Only one function at any given time can have access to memory and that is either the program, interrupts, the real-time clock, or the DMA, or DMC.

Interrupts

A multilevel interrupt facility provides simple but efficient supervision of processing involving combinations of input/output and computing. This facility allows branching as necessary between a main program and servicing routines for all input/output devices and for internal central processor conditions. It eliminates the need for programmed tests to detect the completion of input/output operations. A flexible interrupt capability has important applications in the field of data communications and other real-time areas but it is equall applicable to the supervision of operations as universal as reading and punching cards or reading and writing magnetic tape.

Interrupts in the 716 are classified in two groups: controlled and privileged. The source of a controlled interrupt is a peripheral device control in the I/O system (i.e., 316/516-compatible interrupts or standard 716 I/O bus interrupts). Privileged interrupts are caused by internal conditions in the central processor (e.g., stack overflow/underflow, trace, power failure, or real-time clock).

Controlled interrupts are enabled and disabled by the ENB and INH instructions, respectively. Since privileged interrupts must inform the system about critical conditions within the central processor, such as power failure, they have a higher priority than controlled interrupts and are not affected by ENB and INH instructions.

A controlled program interrupt occurs whenever a peripheral device has completed an input/output operation. For example, an interrupt occurs at the end of data transmission in a tape read or write operation. Likewise the receipt of a character from a remote station by a communication control may be signalled by a program interrupt. Interrupts from a particular peripheral control can be allowed or inhibited by a privileged program as necessary.

A program interrupt is accompanied by (1) automatic storage of the interrupted program's location and (2) automatic identification of the interrupt by branching to a routine whose address was previously loaded by program into a dedicated memory location. This routine can then service the device that caused the interrupt.

Data Storage Formats in Main Memory

The basic addressable unit of storage in main memory is the 16-bit word. This is also the basic unit of information transferred between main memory and the central processor's A-register. Essentially, there are two types of words -- data and instruction -- each of which can be further categorized. As shown in Figure 7, the contents of a 16-bit *data word* can be interpreted in any of the following ways:

- A 16-bit piece of data,
- Two 8-bit bytes of data,
- A single-precision fixed-point number,
- Half of a single-precision floating-point number,
- Half of a double-precision fixed-point number, or
- Part of a double-precision floating-point number.

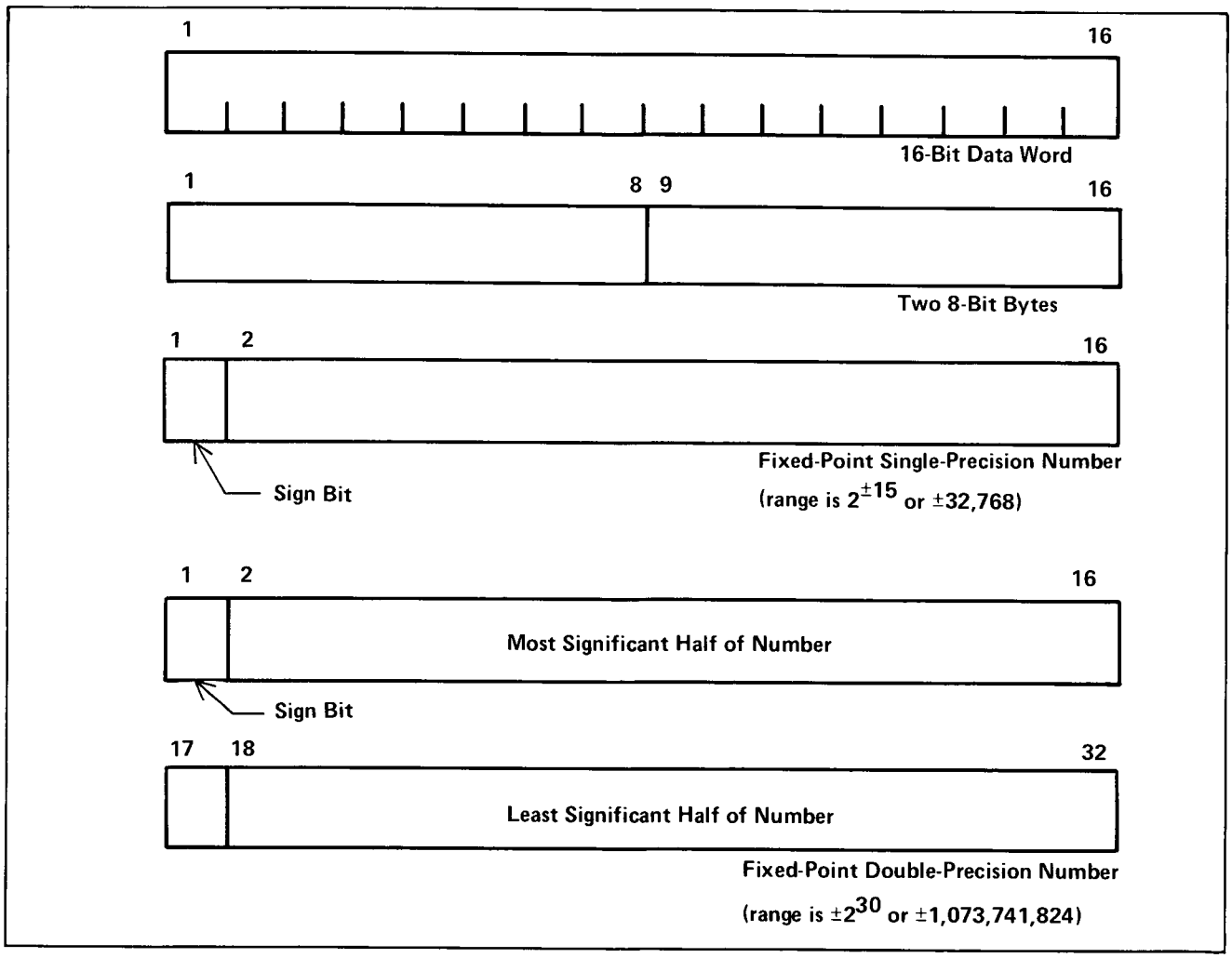


Figure 7. Data Word Storage Formats

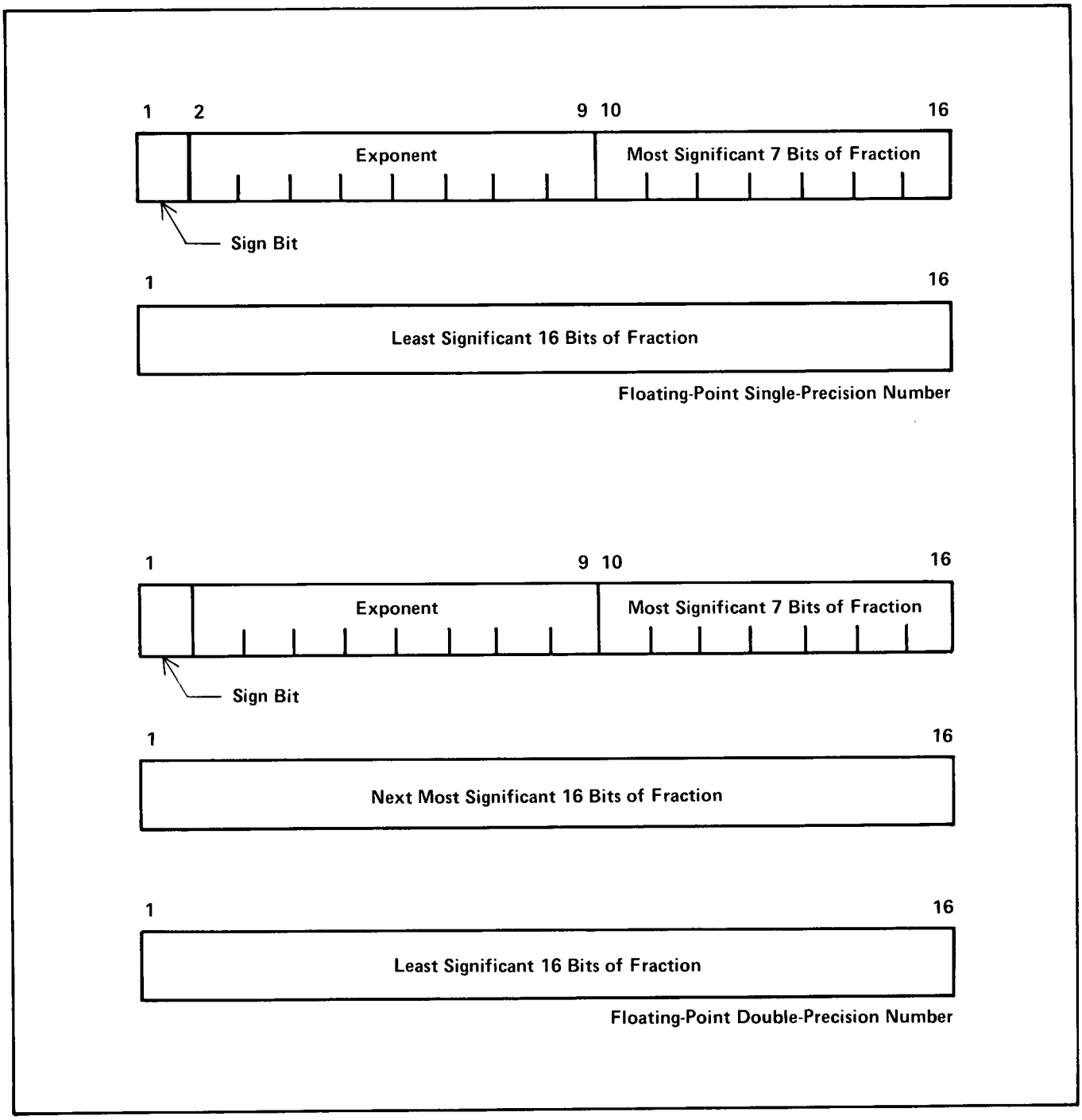


Figure 7 (Cont.) Data Word Storage Formats

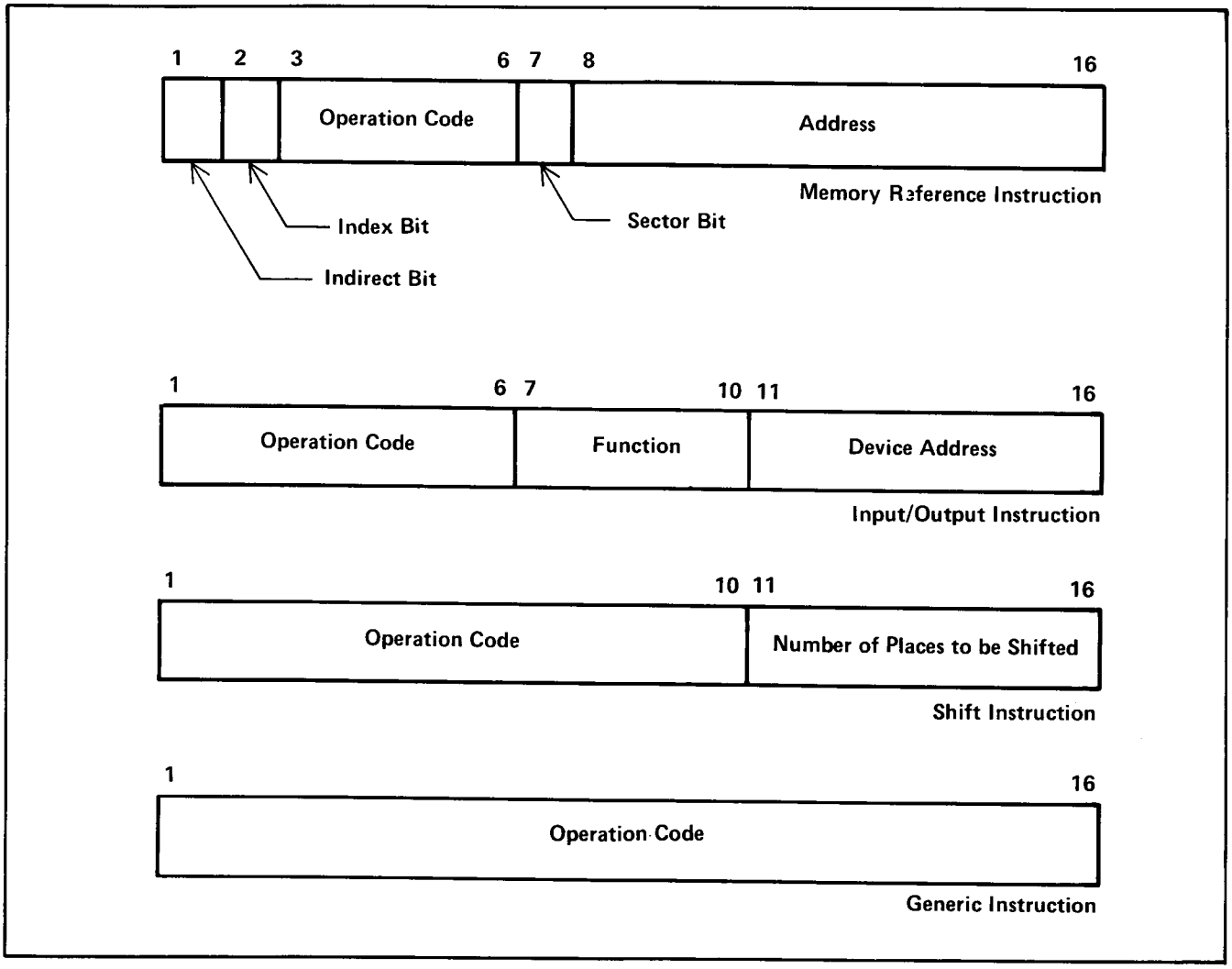


Figure 8. Instruction Word Storage Formats

Instruction Storage Formats in Main Memory

As shown in Figure 8, the contents of a 16-bit *instruction word* can be interpreted as any of the following types of instructions:

- A memory reference instruction – for storing or retrieving data from memory.
- An input/output instruction – for transferring data to or from input/output devices.
- A shift instruction – for movement of data in the A- and B- registers.
- A generic instruction – for any type of operation not mentioned above.

Addressing

For addressing purposes, memory is divided into 512-word sectors. The processor can directly address 1,024 word locations: the base sector (the first 512 locations of main memory) and the currently executing sector (the memory area to which the program counter currently points). All of main memory can be addressed indirectly or through the use of an index register. Two additional addressing modes are standard: general register and stack. The address bits of a memory reference instruction determine the addressing mode.

INDIRECT ADDRESSING

For all instructions that permit indirect addressing, the chain can continue indefinitely; i.e., it is multilevel. An indirect address can be either pre- or post-indexed. When indirect addressing is required, the effective address is assumed to be in the location specified by the address portion of the instruction and the selected sector address. However, if this location also calls for indirect addressing, an additional memory cycle is initiated. Indirect addressing adds 775 nonoseconds per level to the instruction execution time.

INDEXED ADDRESSING

When the index bit of an instruction is set, the contents of the index register are added to the direct address of the instruction to produce an effective address. If indexing is specified in the instruction word, it occurs before any indirect addressing; if specified in an indirect address, it occurs after indirect addressing. Most importantly, no additional cycles are required for instruction execution[1] when indexing.

EXTENDED ADDRESSING

With extended addressing, the indirect address format includes 15 address bits in order to access more than 16K words of memory; indexing is specified in the instruction and is applied after indirect addressing.

GENERAL REGISTER AND STACK REGISTER ADDRESSING

For programming flexibility, two additional addressing modes are standard: register and stack. These modes allow the programmer to address registers as if they were memory locations.

READ-ONLY MEMORY

Like main memory, ROM has a storage format of 16-bit words and its cycle time is 775 nanoseconds. Addressing overlay, a ROM feature, ensures that with the addition of the ROM no addressing capabilities or main memory storage are sacrificed. It allows read access to ROM via the same addressing circuitry used for accessing main memory.

A 2,048-word ROM is included with each of the System 700 remote concentrators. ROM is optional for other System 700 configurations. On the remote concentrators, ROM facilitates unattended operation by allowing down-line bootstrap loading of the 716 processor by the main (host) computer. It also provides for transmission of status information to the host.

ROM is programmed ("wired") by Honeywell and cannot be field-modified. When a Model 73050 Remote Message Concentrator is configured at the factory, ROM is programmed according to a standard Honeywell loader. For all other models, ROM is wired according to customer-designed programs.

[1] Except for the JUMP instruction.

OPTIONAL PROCESSING CAPABILITIES

Parity for Main Memory

With main memory parity, two additional bits are provided for each word in main memory. Parity is generated on all memory write cycles and checked on readout. Detection of a parity error causes a parity-error indicator to be set. The indicator can be tested under program control. Setting of the indicator can also cause a program interrupt. Feature 1202 provides parity for the first 4K words of main memory; Feature 1203 provides parity for an additional 4K words of memory.

When parity is installed, the following instructions are added to the standard instruction set:

Op Code	*Description*	*Execution Time*
SMK '20	Set Mask (A-register bit 15 controls parity)	2300 ns
SPS	Skip on Parity Error	775 ns
SPN	Skip on No Parity Error	775 ns
RMP	Reset Memory Parity Indicator	775 ns

Space is reserved in the mainframe for this feature.

High-Speed Arithmetic Package

Feature 2010, High-Speed Arithmetic Package, provides hardware multiply, divide, and normalize and hardware double-precision arithmetic capability, as well as base sector relocation. Ten instructions are added to the standard instruction repertoire with this feature. Space for the 2010 is reserved in the mainframe.

CAPABILITIES

- Extended arithmetic capability – Single-word multiply and divide memory-reference instructions are indexable and indirectly addressable.
- Enhanced floating-point operations – Normalize and Shift Count to A instructions facilitate automatic formatting of mantissa and exponent.
- Hardware-implemented double-precision operations – Add, subtract, load, and store of double-word (32-bit) operands.
- Faster arithmetic library subroutines – e.g., square root is six times faster, arctangent seven times, sine sixteen times

INSTRUCTIONS PROVIDED WITH FEATURE 2010

Mnemonic	*Function*
MPY	Multiply
DIV	Divide
NRM	Normalize
SCA	Shift count to A
DBL	Enter double-precision mode
SGL	Enter single-precision mode
DAD	Double add
DSB	Double subtract
DLD	Double load
DST	Double store

BASE SECTOR RELOCATION

Included with the High-Speed Arithmetic Package is Base Sector Relocation. It allows the base sector for the currently operating program to be relocated from physical sector 0 to any sector. An additional register, the J-register, identifies the physical sector currently assigned as the base sector.

Real-Time Clock and Watchdog Timer

The Type 3000 Real-Time Clock/Watchdog Timer consists of two independent clocks – one controlled by the line frequency, the other controlled by a crystal. Both clocks may be used independently or simultaneously and are always under program control. The time interval is detected through automatic interrupt generation.

The watchdog timer provides a means of detecting system failure by generating an interrupt upon time-out. It can also activate an external alarm.

FEATURES

Once started, the line clock requests an interrupt every 16.67 ms for a 60 Hz line frequency or every 20.0 ms for a 50 Hz line frequency. The clock may be stopped at any time under program control.

The crystal clock provides up to 40.95 ms interrupt periods in 10.0 μs increments. The clock is started with an output instruction which loads the counter and holding register with a 12-bit number. When the counter overflows, an interrupt request is generated and the contents of the holding register are strobed into the counter with the clock continuing to run.

An external input is provided for an external timing source to be used in place of the crystal clock. The crystal clock is disabled via a jumper on the Printed Circuit board. This external input provides for synchronizing computer interrupts to an external clock source, as well as providing for different time intervals between interrupts.

The watchdog timer is preset for 1.25 sec ±200 ms. Once started, the program must retrigger the timer within that time interval. Failure to do so results in the generation of an interrupt to location '55. This interrupt is independent of mask setting, priority interrupt net, and ENB/INH instructions.

Optionally the watchdog timer may be started or retriggered by an external control signal and can signal an external device that a time-out has occurred. When the watchdog timer times out and generates an interrupt, it also activates the external device signal. The watchdog timer may be stopped with an Initialize or Master Clear instruction.

The Real-Time Clock/Watchdog Timer uses one card slot of mainframe space.

INSTRUCTION COMPLEMENT

OCP '1010	Start Watchdog Timer
OCP '1110	Stop Crystal Clock
OCP '1210	Acknowledge (clears interrupt indicators and enables further requests)
OCP '1310	Start Line Clock
OCP '1410	Stop Line Clock
OCP '1510	Set Interrupt Mask
OCP '1610	Reset Interrupt Mask
OCP '1710	Initialize – Clock and Timer Master Clear
INA '1110	Input ID Code
INA '1210	Input Status (indicates which clock interrupted)
OTA '1010	Load and Start Crystal Clock

An external input is provided for an external timing source to be used in place of the crystal clock. The crystal clock is disabled via a jumper on the printed circuit board. This external input provides for synchronizing computer interrupts to an external clock source, as well as providing for different time intervals between interrupts.

Data Multiplex Control Adapter

The Type 3010 Data Multiplex Control Adapter offers full compatibility between a Type 716 Central Processor and Model 316 and 516 peripheral devices and controls. The 3010 consists of two functional parts – the data multiplex control (DMC) part and the input/output adapter part.

The DMC portion of the 3010 is program-compatible with the standard Model 316 DMC, the 316 high-speed DMC, and the Model 516 DMC. It includes a DMC autoswitch, which enables a peripheral control to transfer large blocks of magnetic tape data, without gaps, at high speeds.

The I/O adapter portion of the Type 3010 transfers data between the A-register in the Type 716 Central Processor and peripheral device buffer registers in the 316-/516-compatible peripheral controls. This portion of the 3010 also handles information required for operation of the peripheral controls. It operates under the System 700 I/O instructions (OCP, SMK, INA, OTA, and SKS).

Included with the Type 3010 is a separate special logic drawer, which houses a portion of the 3010 logic and up to eight peripheral controls[1]. Up to three additional logic drawers can be added. Each additional drawer accomodates up to eight additional peripheral controls; thus, a maximum of 32 316-/516-compatible peripheral controls can be connected to the 3010. Additional drawers are provided with packaged System 700 models as required at no additional charge. Cables from the additional drawers plug into the first logic drawer. The 3010 is a wire-wrapped board that occupies the first two card slots in the I/O bus drawer of the Type 716 Central Processor.

System 700 peripheral devices that require the use of a DMC Adapter are as follows:

Type	*Description*
4021	7-Track Magnetic Tape Subsystem
4150	9-Track Magnetic Tape Subsystem
4720	Removable Disk Storage Subsystem
5121	Card Reader
5140	Card Reader/Punch
5520	Printer

[1] The number of peripheral controls that can be installed in a drawer depends on the types of peripherals selected.


Honeywell 720

4

THE PERIPHERALS: A WIDE CHOICE FOR SYSTEM 700

Available to the System 700 user is an array of peripherals that meet all the requirements of a minicomputer's likely applications. The complete choice of input/output devices (see Table 5) permits an equally complete choice of data recording media and data entry methods.

In addition to the peripherals described in this section, various analog and digital input/output modules are available for the unique applications of sensor-based systems.

A mandatory requirement of many communications applications, such as inquiry and message switching, is fast access to stored information. Core memory, of course, provides the fastest access possible. But for large files, memory is expensive, and other media must be considered. As shown in Table 5 magnetic tape equipment and disk storage are available in various configurations and capability levels designed to match specific user requirements. The complete line of teletypewriters offers an effective means of implementing a man/machine interface for system control functions. Other peripherals fulfill the need for file storage and a variety of input/output capabilities.

System 700 peripherals will be supported by the OS/700 Executive. A Test and Maintenance Program will be provided with each device to assist in maintaining and repairing the equipment.

DISK STORAGE SUBSYSTEMS

Removable Disk Subsystem

The Type 4720 Removable Disk Subsystem provides high

TABLE 5. PERIPHERAL EQUIPMENT AVAILABLE FOR SYSTEM 700

	You can order this peripheral equipment in the maximum quantities shown below:								
If you have a Model:	Console Teletype-writer	Paper Tape Reader	Paper Tape Punch	Card Reader[a] or Card Reader/Punch[a]	Printer[a]	Magnetic Tape[a] 7-Track	Magnetic Tape[a] 9-Track	Fixed-Head Disk Subsystem	Removable Disk Subsystem[a]
72001 Terminal System	8	1	1			2 or	2		
72002 Peripheral System	8	1	1	1	1	4 or	4	2 units (one million words)[b]	2 drives (15 million words)[b]
72020 Sensor-Based System	6	1	1			2 or	2		
72021 Sensor-Based System	6	1	1			2 or	2	2 units (one million words)	
72050 Remote Concentrator Line	1							2 units (one million words)	
73050 Remote Message Concentrator	1								

[a] A Type 3010 DMC Adapter is required if this type of peripheral is installed. One such adapter per central processor services all peripherals that require DMC control.

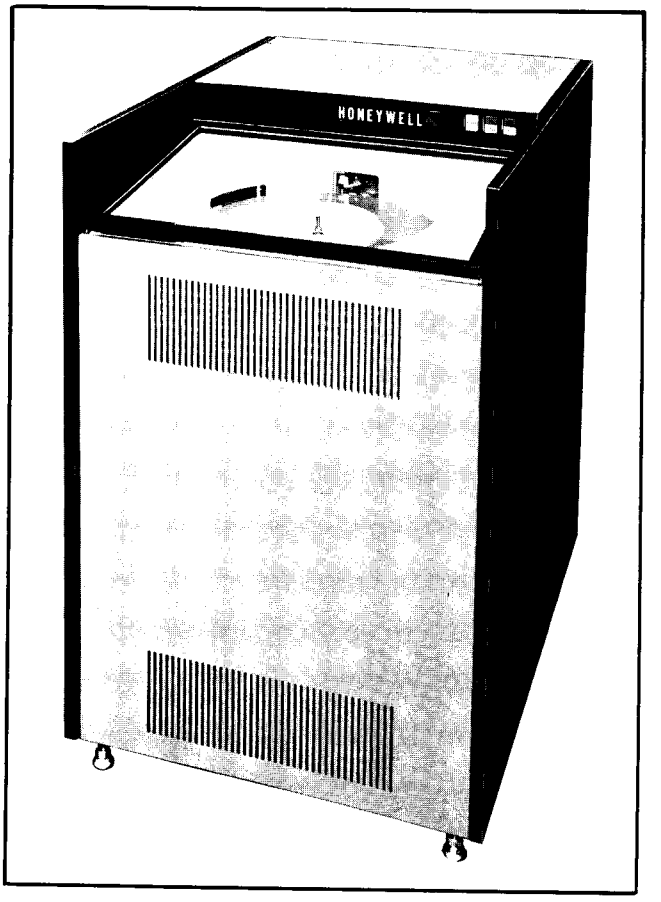
[b] Either a fixed-head disk subsystem or a removable disk subsystem can be selected.

storage capacity (by the use of removable disk packs) and low access time. Each disk pack contains 20 usable recording surfaces. Low access time results from the use of 20 read/write heads mounted on a movable access arm that is positioned under program control.

The basic 4720 includes a disk control and one disk pack drive that stores 7.5 million 16-bit words. The basic disk control can be connected to as many as four disk pack drives. The control can be expanded to handle a total of eight disk pack drives by the addition of Feature 4703, Expansion of Disk Control. By the addition of Type 4721 Additional Disk Pack Drives, the basic storage capacity of 7.5 million words can be expanded to a full capacity of 60.0 million words in increments of 7.5 million words.

Subsystem features are as follows:

- Removable disk packs allow the drives to operate with different packs as on-line storage requirements change.
- Direct seek is standard. This permits track-to-track head movement without returning to the base position.
- A single seek command positions the read/write heads to operate with up to 36K words stored on 20 tracks.
- A seek-complete interrupt prevents loss of processing time during the seek operation.
- Program-controlled tests for data transfer or transfer setup errors are available.
- Up to eight disk pack drives can be connected, permitting modular expansion of the system.
- Variable track formats permit the storage of records of variable length.
- A write lockout capability protects storage areas.
- Central-processor-finished indication permits on-line disk pack removal in multidrive systems.



Removable Disk Subsystem

Fixed-Head Disk Subsystems

Of all the System 700 peripheral equipment available, the fixed-head disk subsystems offer the fastest access to stored information. Low access time is achieved by using a read/write head per recording track. The average access time is 12.5 milliseconds, and the average data transfer rate is 82,000 words per second.

Features of the teletypewriter include the following:

- Printing and paper tape reading and punching – in both on-line and off-line modes.
- On-line operation in full-duplex mode.
- Operation in two modes: normal and Series 16 compatible.

COMMUNICATION LINE CONTROLLERS

Single-line and multiline controllers enable the System 700 models to receive and transmit data over switched and private communication lines. The controllers offer a selection of lines and speeds and compatibility with many types of terminals and systems (see Tables 6 and 7).

Instructions are provided to allow software control in the following major areas of operation of the LSMLC: gross control of functions, data transfer control, and maintenance/troubleshooting aids.

A software package, controllable by an executive, will operate the controllers. The package is modularly struc-

TABLE 7. SELECTED TERMINALS USED WITH COMMUNICATION LINE CONTROLLERS

Terminal	Speed	Data Set[a]	Operation	Controller Type
Model 28 Teletypewriter	60-100 Words/Min	103F 103A	FDX FDX or HDX	6333
Model 33/35 Teletypewriter	60-100 Words/Min	103F 103A	FDX FDX or HDX	6333
Model 37 Teletypewriter	150 Words/Min	103F 103A	FDX FDX or HDX	6333
Kleinschmidt 311/321 (ASCII Models)	Up to 136 Words/Min Up to 272 Words/Min	103A 103F	FDX or HDX FDX	6333
IBM 1050	14.8 Char/Sec	103A/F	HDX	6333
Honeywell Data Station	120 Char/Sec 180 Char/Sec	202C 202D	HDX HDX	6333
Honeywell Keytape[b], Keyplex[b]	120 Char/Sec 180 Char/Sec	202C 202D	HDX HDX	6333
Honeywell VIP 765, 775, 785	300 Char/Sec	201B	HDX	6312, 6321, 6322
Raytheon DIDS-400	120 Char/Sec 300 Char/Sec	202C 201B	HDX HDX	6333 6312
Sanders 720 Data Display System	250 Char/Sec 300 Char/Sec	201A 201B	HDX FDX	6312
Honeywell Series 200/2000	250 Char/Sec	201A	HDX	6312
Computer with 281 Controls or DATANET[b] 2000	300 Char/Sec	201B	HDX	
IBM 360 with 2701 Synchronous Adapter Type 1	300 Char/Sec	201B	HDX	6312
Other System 700 Computers	300 Char/Sec	201B	FDX or HDX	6312 and others

[a]Bell System model numbers are listed. Equivalent data sets can be interfaced.
[b]Trademark.

Paper Tape Punch

The Type 5210 Paper Tape Punch allows the recording of information, at a rate of up to 110 characters per second, onto paper tape. The punch not only provides a means of recording data blocks for later processing, but also prepares program tapes for computer operations and maintenance.

The Type 5210 has the following features:

- A maximum transfer rate of 300 characters per second.
- A separate cabinet locatable up to 25 feet from the computer.
- A control unit in the mainframe expansion drawer.
- Control and interrupt logic supporting both normal- and compatible-mode software.
- Single-character start/stop control to allow a variable input block size and gapless blocks.
- A photocell sensing system.

TELETYPEWRITERS FOR ON-SITE OR REMOTE USE

The teletypewriters available with System 700 central processors are the Type 5307 (ASR-33), 5310 (KSR-33), and 5507 (ASR-35). Types 5307 and 5507 are similar in operation and specifications; however, Type 5507 is a heavy duty unit for usage exceeding two or three hours per day.

All teletypewriters print data from the central processor or transmit data to the central processor at the rate of ten characters per second. Types 5307 and 5507 can also read and punch paper tape at the same character rate. Type 5310 does not read or punch paper tape.

The teletypewriter control contains two 8-bit data registers for full-duplex operation. The data transfers between the control and the central processor are bit-parallel. The control can operate in two modes, normal (which supports System 700 software) and compatible (which supports Series 16 software).

TABLE 6. COMMUNICATION LINE CONTROLLERS AVAILABLE FOR SYSTEM 700

	You can order these communication controls in the maximum quantities shown below:								
If you have a Model:	6312 Synchronous Single-Line Controller (for one line)		6333 Multifunction Multiline Controller (for up to 8 synchronous and 8 asynchronous lines, or for up to 16 asynchronous or 16 synchronous lines)		6322 Universal Multiline Controller (for up to 64 synchronous and/or asynchronous lines)		6321 Low-Speed Multiline Controller (for up to 128 asynchronous lines)		
Model 72001 Terminal System	2	or	1		–		–		
Model 72002 Peripheral System	2	or	1		–		–		
Model 72020 Sensor-Based System	–		1		–		–		
Model 72021 Sensor-Based System	–		1		–		–		
Model 72050 Remote Line Concentrator	4		2		–		–		
Model 73050 Remote Message Concentrator	4		2		1	or	1		

[a] Either two single-line controllers or one multiline controller.

[b] Either a universal multiline controller or a low-speed multiline controller.

- Identifies error cards by offset-stacking under program control.
- Provides interrupt operation for real-time environment.
- Includes full set of operator controls and indicators.

Card Reader/Punch

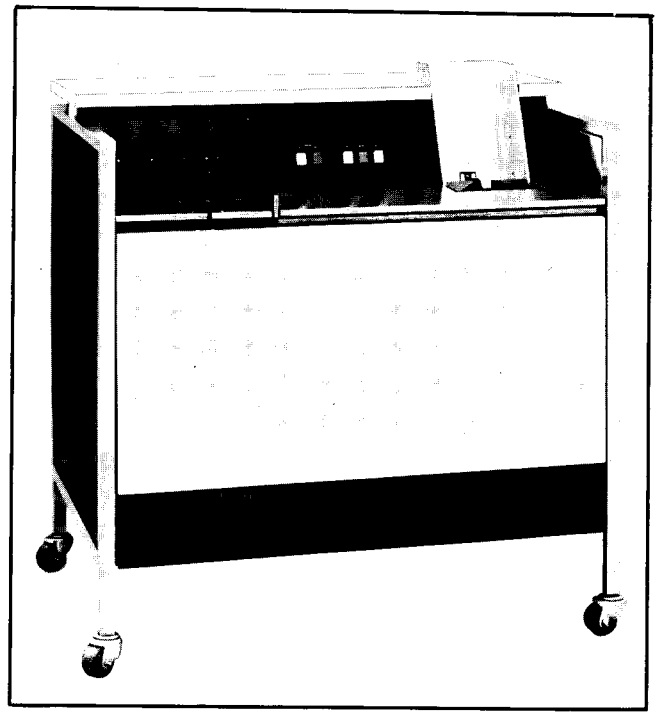
The Type 5140 Card Reader/Punch operates at up to 400 cards per minute in either read or punch mode. A 12-bit register buffers data transfers in either mode; the register temporarily stores the contents of one card column.

Data sensing is accomplished by a photoelectric system which reads either alphanumeric or binary punched cards on a column-by-column basis. In the alphanumeric mode, the reader accepts cards punched in the conventional Hollerith code. Automatic hardware code conversion produces a 6-bit BCD representation of the data in each column. In the binary mode all 12 rows of a column are read as a 12-bit word.

The punch mechanism operates in a binary mode to output data, column-by-column, on the cards. The punch speed is 100 to 400 cards per minute.

The Type 5140 has the following features:

- Reading and punching capabilities in a single device.
- Data reading and additional data punching on the same card in one pass.
- Alphanumeric or binary data reading on programmed command.
- Hardware code conversion from Hollerith to 6-bit BCD code.
- Error card identification by offset-stacking under program control.
- Program-controlled card punching, 100 to 400 cards per minute.
- A dual card punching mechanism, to increase card throughput.
- Interrupt operation for a real-time environment.
- Error detection via interrupt, status word, and test commands.
- A full complement of operator controls and major function indicators.



Card Reader/Punch

PAPER TAPE EQUIPMENT

Paper tape equipment available includes the Type 5010 Paper Tape Reader and the Type 5210 Paper Tape Punch. Each of these devices includes the required control logic for interfacing with a System 700 central processor. The one-inch-wide tape can be paper, mylar-based, or a combination of the two.

Paper Tape Reader

The Type 5010 Paper Tape Reader allows a Type 716 Central Processor to input data punched on tape. The reader is a high-speed input device for loading source programs, object programs, and data. It operates at 300 characters per second. Its features include the following:

- A maximum transfer rate of 300 characters per second.
- A separate cabinet locatable up to 25 feet from the computer.
- A control unit in the mainframe expansion drawer.
- Operation in two modes: normal (System 700) and Series 16 compatible.
- Control and interrupt logic supporting both normal- and compatible-mode software.
- Single-character start/stop control, to allow a variable input block size and gapless blocks.
- A photocell sensing system.

Error Correction, is optional. Up to three additional Type 4153 Magnetic Tape Units can be connected to a 4150 Subsystem.

Features are as follows:

- Priority interrupt operation for real-time environment.
- Write-enable ring for file protection.
- Data transfer rates up to 28,800 bytes per second.
- Full set of operator controls and indicators for major functions of the device.
- Read-after-write error checking, lateral parity, longitudinal redundancy character, cyclic redundancy character.
- Simultaneous rewind of multiple tape units.
- Compatibility with systems which satisfy IBM and ANSI NRZI recording formats.

PRINTER

The Type 5520 Printer is a fully buffered, printed copy output device that operates at 300 lines per minute. Its line width is 120 characters per line (optionally 132 when Feature 5511 is installed).

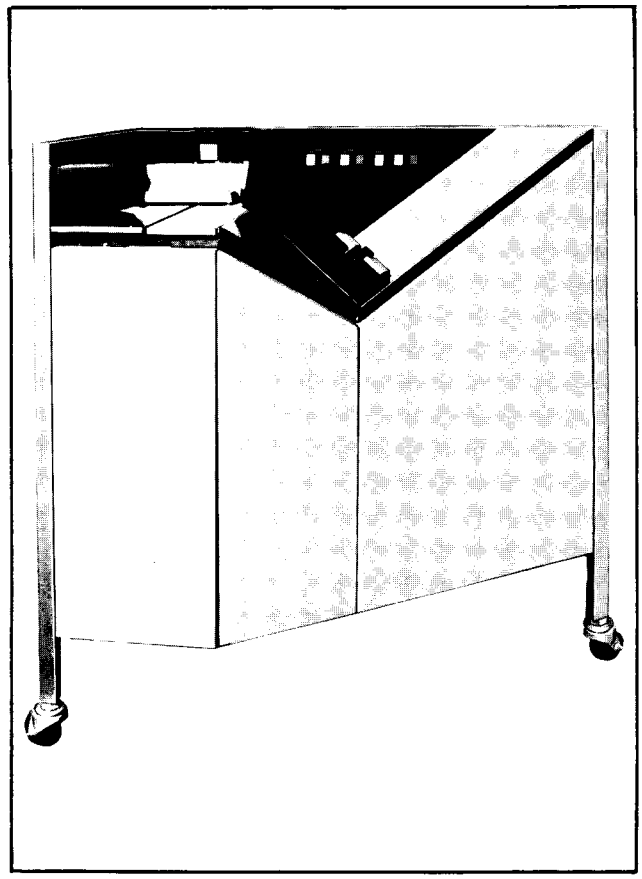
The Type 5520 consists of a freestanding printing device and a control (containing the computer interface logic and buffer memory) which is housed in the computer mainframe or expansion drawer. The buffer memory element is a solid state, sequential-access random-time unit.

The Type 5520 has the following features:

- The rotating print drum contains a full set of 63 symbols (plus blank) to be printed in any of the 120 or 132 print positions on a line.
- The drum is a swingaway type, to facilitate form and ribbon loading.
- Its surface is of hardened steel, to eliminate type wear and ensure sharp, clear printing.
- Integral maintenance panels and off-line test modes ease checkout and servicing operations.
- A position servo paper feed system increases reliability.
- The control utilizes a 120- or 132-character FET buffer memory for data transfer.
- Complete solid-state control circuitry offers proven reliability.

UNIT-RECORD EQUIPMENT

Two unit record peripherals are available for System 700: the Type 5121 Card Reader and the Type 5140 Card Reader/Punch.



Card Reader

Card Reader

The Type 5121 Card Reader is an 800-cards-per-minute input device operable with System 700 central processors. Data sensing is accomplished by a photoelectric system which reads either alphanumeric or binary punched cards on a column-by-column basis. The reader is completely buffered in either data mode by the use of a 12-bit register which holds all data from one column.

In the alphanumeric mode, the reader accepts cards punched in conventional Hollerith code. Automatic code conversion produces a 6-bit BCD representation of the data in each column. In binary mode, all 12 rows of a column are read as a 12-bit word.

Features are as follows:

- Reads punched cards containing either alphanumeric or binary data upon programmed command.
- End-feeds and reads cards column-by-column.
- Reads cards photoelectrically, 800 cards per minute maximum.
- Provides automatic hardware code conversion in alphanumeric mode, Hollerith to 6-bit BCD code.
- Simplifies program timing considerations by demand feeding.

Each subsystem consists of a disk control and a disk storage unit. System 700 fixed-head disk subsystems are available in the following configurations:

Type	*Storage Capacity*
4510	64K words
4511	128K words
4512	256K words
4513	512K words

An optional Type 4514 Disk Storage Unit provides an additional 512K-word capacity for the Type 4513. In addition, Feature 4516[1], Inert Gas, is available for all System 700 fixed-head disk subsystems.

Features of the subsystems include the following:

- One read/write head per track provides for fast access time.
- The data transfer rate is 82,000 words per second.
- Capacity is expandable to one million words per subsystem.
- Write lockout is controllable by eight switches. Each switch controls four tracks (16K words).
- An interleaved data format structure is used.
- Extensive error detection includes bus parity and a polynomial check byte for each sector of data.
- The disk control transfers operation and diagnostic status for error checking.
- Front access provides ease of maintenance.
- Direct Memory Access (DMA) is used for data transfers.

MAGNETIC TAPE EQUIPMENT

Two magnetic tape subsystems are available for System 700 configurations: the Type 4021 7-track Magnetic Tape Subsystem and the Type 4150 9-track Magnetic Tape Subsystem. As a basic configuration, each subsystem consists of one tape unit and a tape control.

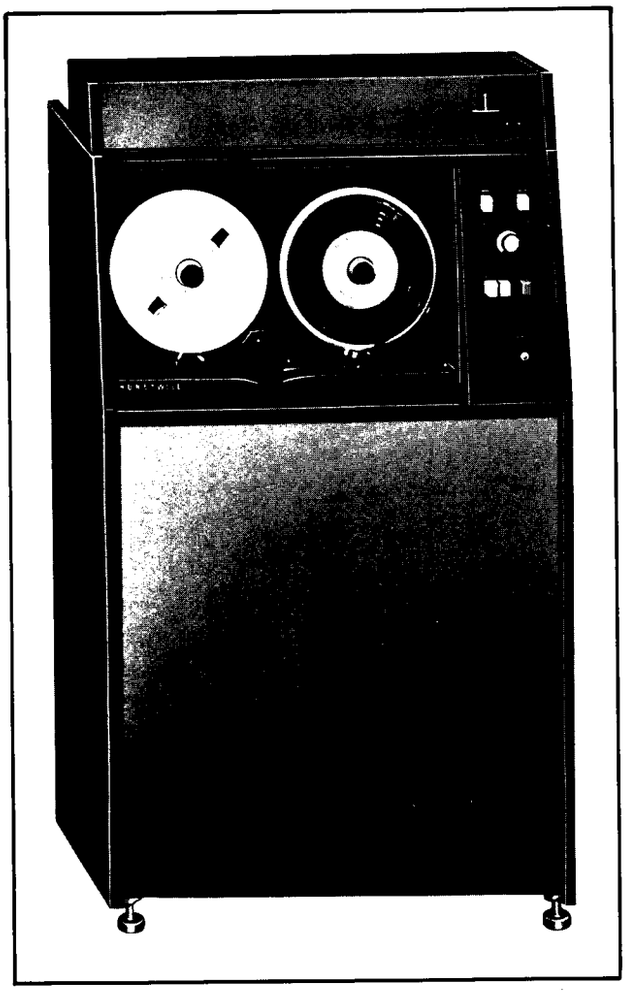
7-Track Magnetic Tape Equipment

The Type 4021 operates at up to 26 inches per second and at standard recording densities of 200, 556, and 800 bpi. This subsystem is IBM-code-compatible in the two-character-per-word mode of operation. The 4021 Subsystem can be expanded by the addition of up to three Type 4022 Magnetic Tape Units.

[1]Feature 4516 requires an additional seven inches of vertical rack space to house the gas container. The space is sufficient for two gas containers.

Features of the equipment include the following:

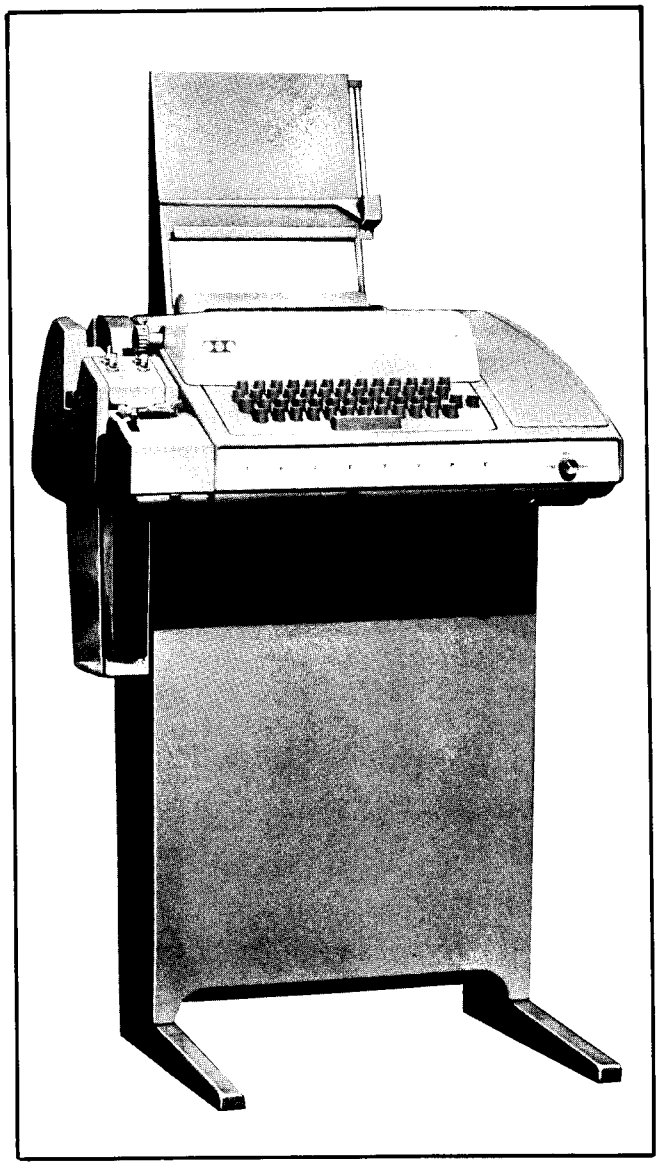
- The nonrecoverable error rate will not exceed one in 10^9 bits.
- Data transfer rates range up to 20,800 characters per second.
- Parity is provided for each character written on tape.
- Multiple-unit rewind.
- BCD or binary word formats are program-selectable.
- The equipment is compatible with all systems that satisfy IBM requirements for NRZI recording.
- Format and amplitudes are compatible with those of IBM 729 series tape units.



7-Track Magnetic Tape Unit

9-Track Magnetic Tape Equipment

The Type 4150 9-track Magnetic Tape Subsystem operates at up to 36 inches per second and at a recording density of 800 bpi. In this subsystem, the tape unit reads and writes compatible, interchangeable tapes that satisfy IBM and ANSI requirements for NRZI format. Feature 4151, Read



Type 5307 Teletypewriter

tured so that appropriate sections can be put together to address a certain application. Moreover, interfaces are such that user application programs may be added easily.

Synchronous Single Line Controller

The Type 6312 Synchronous Single-Line Controller (SSLC) is used to interface a synchronous data communication line through a compatible Bell 201 or 203 Data Set with the Type 716 Central Processor. It can operate in half- or full-duplex mode and can handle transmission rates of up to 10,800 bits per second. Double-buffered, it is designed to translate between synchronous serial bit stream format data and parallel format data. The SSLC uses the programmed input/output (PIO) and interrupt features of System 700. It comes equipped with a 30-foot cable for connection to the data set.

The Type 6313 Code Convention Option enables the SSLC to operate with less overhead in certain situations by including character and character sequence detection, and CRC/LRC check and generation in the hardware. This relieves the software of having to perform these functions.

FEATURES

- Two-way simultaneous operation.
- Hardware synch, character and character sequence detection, and identification.
- Transmit and receive parity controls.
- Longitudinal (LRC) or Cyclic (CRC) Redundancy Checks.
- Support of Transparent Mode Transmission.
- Software control and status of data set signals.
- Built-in maintenance aids.
- MSI technology, TTL logic.
- Versatile software package for general applications.
- Auto-Answering capability.
- Plug-selectable 6-, 7-, or 8-bit code.

SOFTWARE CONSIDERATIONS

The line discipline is contention establishment and termination and transparent message transfer. These categories correspond closely to Binary Synchronous Communications (BSC). The discipline requires "handshaking" to establish a master-slave relationship and to assure validity of data transmission between both ends of the communication line connected to the SSLC. Prior to establishment of transmission, either end may bid for master status. When one end obtains master status, the other becomes slave. Data is thus transmitted from master to slave until terminated by End of Transmission (EOT); either end may then bid for master status. Positive or negative acknowledgments are transmitted by the slave for every message block received, to indicate that it was received correctly or not.

A block check character is calculated and transmitted by the SSLC for every transmitted message block and calculated and checked for every received message block, to determine whether the message is correct or should be retransmitted.

Multiline Controllers

LOW-SPEED MULTILINE CONTROLLER

The Type 6321 Low-Speed Multiline Controller (LSMLC) interfaces multiple data communication lines to the Type 716 Central Processor. A character-oriented device, it assembles bit serial data into characters for input to the processor, and disassembles parallel data into bit serial data upon output from the processor.

Features

- Capacity to interface 128 narrow-band communication lines.
- Ability to handle mixed terminal speeds (45 to 300 baud), jumper-plug-configurable.
- Transfer rate of 11,000 characters per second.
- Ability to handle mixed line parameters, such as speed, code length, number of stop bits, and parity sense, jumper-plug-configurable.
- Modular expansion of line modules in groups of four lines.
- Software control and interrogation of data set signals.
- Built-in maintenance aids (line looping, etc.).
- MSI technology, TTL logic.
- Low line-handling requirements on processor, resulting from increased use of external integrated memory.

Basic Configuration

The LSMLC system consists of two main elements:

- A 128-line multiplexer (communications controller).
- Line modules, each of which interfaces four 103A or 103F modems.

The basic system may be summarized as follows:

Type	*Description*
6321	Low-Speed Multiline Controller: includes I/O bus buffer board, two high-performance cables, and multiplexer.
6351	103 Line Module: interfaces four 103A or 103F modems to LSMLC. Includes 30-foot modem cable.

Characteristics

Capacity: From 4 to 128 channels; expandable in groups of 4 channels (line module).

Transmission Type: Half- or full-duplex.

Transmission Mode[1]*:* Asynchronous, with speeds from 45 to 300 baud. Six speeds, jumper-selectable per line module, from following: 45.45, 50, 56.88, 61.1, 66.7, 74.2, 75, 110, 133.3, 134.5, 148.4, 150, 200, 300.

Data Format[1]*:* Code length, configuration-plug-selectable: 5, 6, 7, or 8 bits, per line module. Stop bits, configuration-plug-selectable: 1, 1.42, or 2, per line module.

Parity[1]*:* Checked on incoming data lines and generated for outgoing data lines. Sense: even, odd, or none; configuration plug-selectable per line module.

Interface: Line module output is plug-compatible with Bell 103A and 103F Data Sets. Conforms with EIA RS232C specifications.

Data Set Signal Control and Status: Allows setting of Data Terminal Ready, under software control. Allows interrogation of Carrier Detect and Data Set Ready under software control.

MULTIFUNCTION MULTILINE CONTROLLER

The Type 6333 Multifunction Multiline Controller (MFMLC) is used for interfacing asynchronous and synchronous data communication lines with the central processor. The MFMLC can accommodate up to 16 lines by the use of line units; each unit accommodates two lines. The Type 6362 Asynchronous Line Unit handles line speeds up to 2400 baud. Line parameters such as speed, character size, and parity sensing are program selectable with this unit. The Type 6363 Synchronous Line Unit handles line speeds up to 9600 baud. Up to eight units in any combination can be connected to the MFMLC.

UNIVERSAL MULTILINE CONTROLLER (73050 only)

The Type 6322 Universal Multiline Controller (UMLC) interfaces multiple asynchronous and/or synchronous data communications lines to the Type 716 Central Processor. A character-oriented device, it assembles bit serial data into characters for input to the processor and disassembles parallel data into bit serial data upon output from the processor.

Features

- Capacity to interface 64 data communication lines.
- Ability to handle asynchronous and synchronous line mixes:
  Asynchronous: 45 to 2400 baud.
  Synchronous: Up to 10,800 baud.
- Transfer rate of 57,600 characters per second.
- Programmable selection of line speeds and other line parameters (character length, parity).
- Synch detection on synchronous lines.
- Error report status for each line.
- Built-in maintenance aids.
- Modular expansion of line modules in groups of two lines.
- MSI technology, TTL logic.
- Low processor burden resulting from increased use of external controller memory.

[1] Speed, data format, and parity sense for each line module group must be specified at the time of order.

Basic Configuration

The UMLC system consists of two main elements:

- A 64-line (maximum) multiline controller (communications controller).
- Line modules, each of which interfaces two 103, 201, 202 or 203 modems.

The basic system may be summarized as follows:

Type	*Description*
6322	Universal Multiline Controller: includes I/O bus buffer board, two high-performance cables, and controller.
6352	Asynchronous Line Module: interfaces two 103 or 202 modems to UMLC. Includes programmable line speed selection and 30-foot modem cable.
6353	Synchronous Line Module: interfaces two 201 or 203 modems to UMLC. Includes 30-foot modem cable.

Program-Controllable Functions

The UMLC is designed in such a way that line parameters of attached lines are software-configurable. This permits either a static or a dynamic UMLC configuration and allows the UMLC system the flexibility of addressing a changing communications environment. The following functions, program-controllable on a per-line basis, are set by using the necessary I/O instructions:

- Type[1] of line: synchronous or asynchronous
- Type of each synch character on syncrhonous lines
- Clock speed on asynchronous lines
- Type of parity: odd, even, or none
- Character length: 5, 6, 7, or 8 bits
- Data speed control: for setting up differential scan mechanism
- Number of stop bits on asynchronous lines: 1, 1.5, or 2 bits

All the control functions for programming a line are contained in the set of internal UMLC memory locations allocated to a line.

In addition to the line configuration facilities mentioned above, the following line control functions are subject to change under program control at any time during the normal operation of the UMLC:

- Last character for transmission
- Transmit parity on/off
- Transmit enable/disable
- Transmit line break
- Strip synch in receive mode
- Receive parity on/off
- Receive enable/disable
- Search for synch enable

All these control functions are also contained in the set of internal UMLC memory locations allocated to line control. These locations may be addressed by the software by appropriate I/O instructions.

Characteristics

Capacity: From 2 to 64 channels; expandable in groups of 2 channels (line module).

Transmission Type: Half- or full-duplex.

Transmission Mode[1]*:* Asynchronous-speeds from 45 to 2400 baud. Speeds program-selectable from set of eight speeds – 1800, 1200, 600, 300, 150, 75, plus two speeds of programmable value.

Synchronous-speeds up to 10,800 baud. Sync detection – ANSI and EBCDIC synch characters hard-wired; two other synch characters program-controlled. DLE characters: ANSI and EBCDIC DLE characters hardwired; other DLE characters program-controlled.

Data Format: Code length, program-selectable – 5, 6, 7, or 8 bits, per line. Stop bits (asynchronous lines), program-selectable – 1, 1.5 or 2, per line.

Parity: Checked on incoming data lines and generated for outgoing data lines, per software command. Sense: even, odd, or none; program-selectable per line.

Line Control Procedures (Synchronous Lines): Hardware synch character detection provided on synchronous lines.

Hardware strip synch in receive mode (except for transparent mode).

Transmit synch character on underrun with transmit enabled and parity on (non-transparent mode).

[1] This parameter is for internal UMLC purposes; physically different hardware (line modules) are required to interface these two types of lines.

[1] All lines must be configured in pairs as regards type; i.e., if Line 1 is synchronous, Line 2 must be synchronous.

Transmit DLE/SYN on underrun with transmit enabled and parity off (transparent mode).

Transmit mark with transmit disabled.

Interface: Line module output is plug-compatible with Bell 103, 201, or 202 Data Sets. Conforms with EIA RS232C specifications.

Data Set Signal Control and Status:

Asynchronous (Type 6352)
- Data Terminal Ready
- Request to Send
- Transmit Reverse Channel
- Data Carrier Detect
- Clear to Send
- Data Set Ready

Synchronous (Type 6353)
- Data Terminal Ready
- Request to Send
- Data Carrier Detect
- Data Set Ready
- Clear to Send

MODEM BYPASS DEVICES

A Type 6925 or 6926 Modem Bypass provides for communication between a terminal and a Type 716 Central Processor for a distance of up to 2500 feet. The point-to-point configuration is shown in Figure 9. A typical multidrop configuration is shown in Figure 10. The Type 6925 is for synchronous transmission; the Type 6926 is for asynchronous transmission. Both devices handle speeds of up to 10.8 kilobaud.

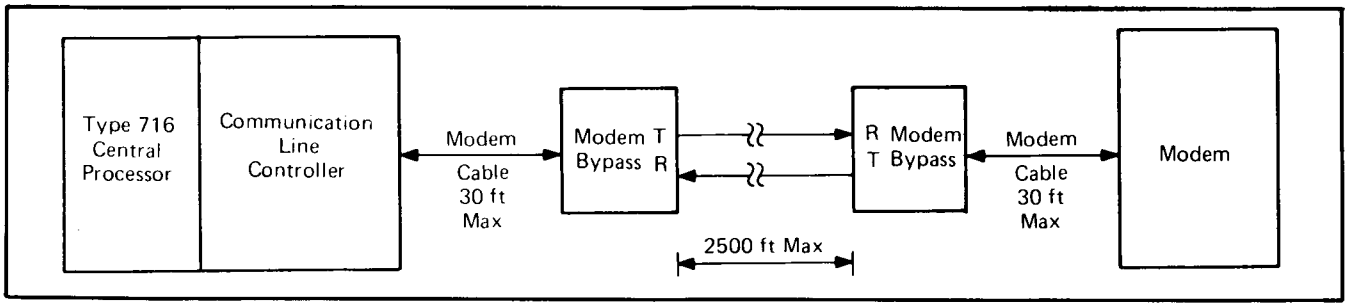


Figure 9. Modem Bypass Point-to-Point Configuration

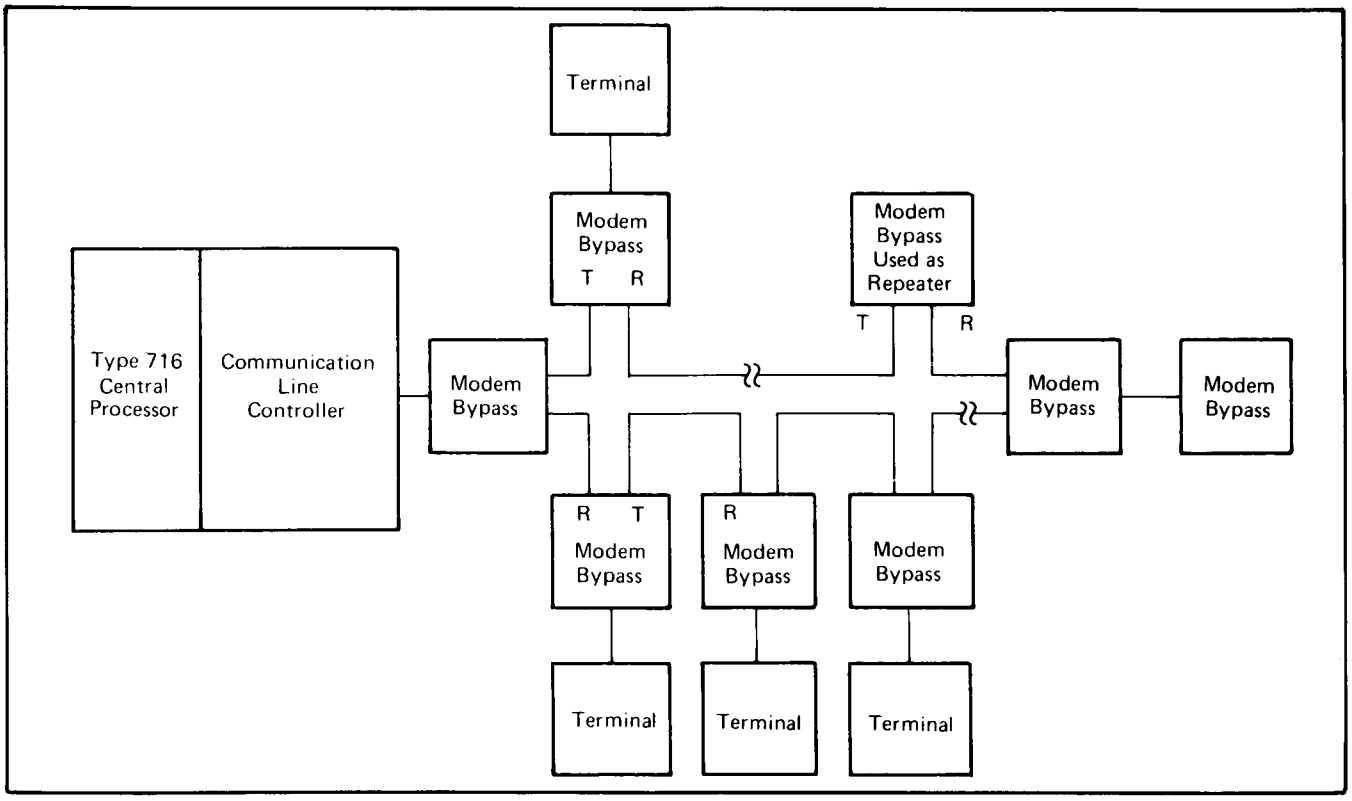


Figure 10. Modem Bypass Typical Multidrop/Repeater Configuration

5

SOFTWARE FOR MAKING THE MOST OF THE MINI

Each System 700 model will be supported by a standard set of software. But add more hardware, and generally more software becomes available. System 700 Software was designed to give the user the programming flexibility that ensures maximum utilization of the hardware. It *makes* System 700 hardware do all the things our engineers *said* it would. Here is the System 700 Software:

- Operating System/700 (OS/700)
- Language Processors, including
  - DAP/700 Macro Assembler
  - BASIC Interpreter
  - Linkage Editor
  - Fortran IV
- Test and Maintenance Routines
- Host-Resident Software System

OPERATING SYSTEM/700

With OS/700's functionally oriented software, the user can design his own software systems according to his specific requirements. OS/700 is designed to accommodate the evolution of software enhancements. Therefore, the system will grow as new software capabilities are made available . . . and without requiring the user to reprogram.

The three basic components (see Figure 11) of OS/700 are:

- OS/700 Executive Components
- OS/700 Subsystems
- OS/700 Module Libraries

OS/700 Executive Components

The OS/700 Executive will provide the software necessary to control the execution of programs in a real-time, multiprogramming environment. The modular structure and flexibility of the Executive system allows users to configure an efficient system for a wide range of capabilities. System configuration involves selecting and linking only those modules applicable to the user's unique requirements.

Some of the features of the Executive system include:

- Multiprogramming – the number of programs active at any one time is limited only by the available memory and the peripheral devices.

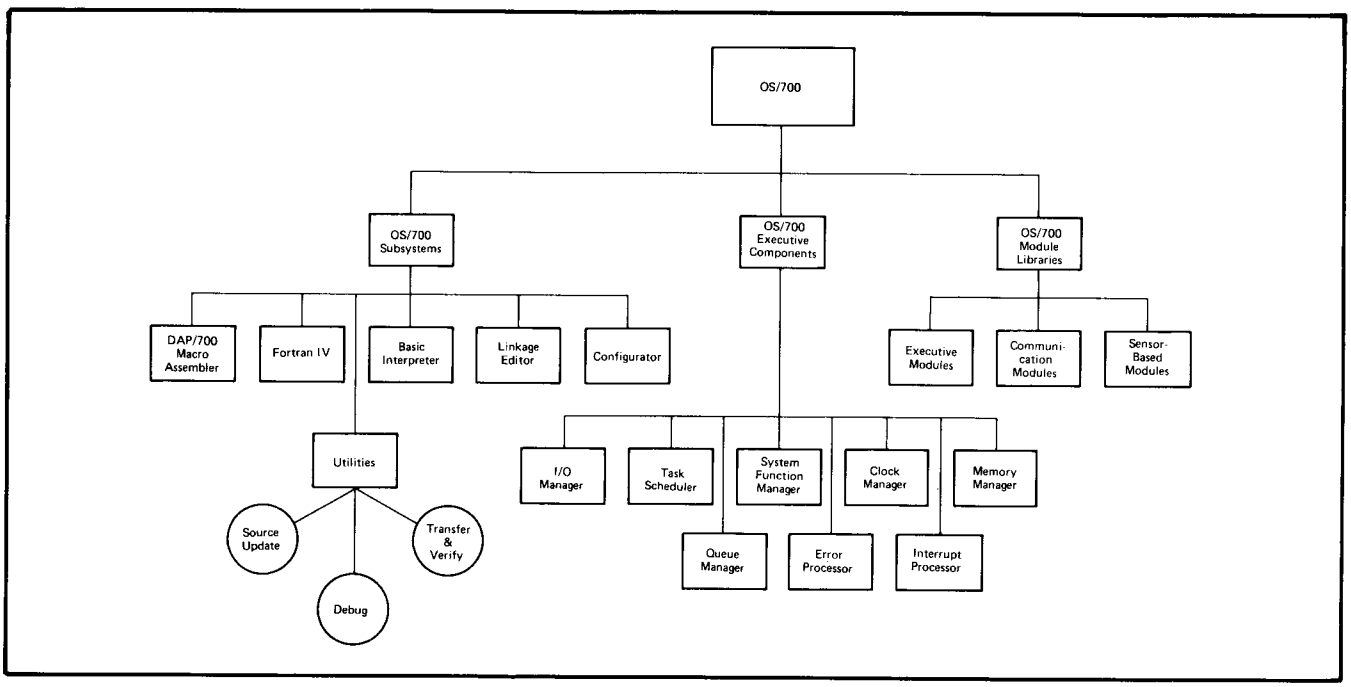


Figure 11. OS/700 Components

- Centralized control of peripheral input/output operations and associated interrupt processing.
- A complete set of utility, support, debug, and peripheral device test programs.
- Computer-to-computer communication for interfacing with large host computers and networks.
- System control for on-line modification and interrogation.
- Task Scheduler – insures that high priority tasks are executed before low priority tasks.
  - When two or more programs bid for execution time, the Executive will initiate the program carrying the highest priority.
  - Multitask scheduling gives a program the capability of initiating several other programs without interrupting its own processor.
- System Function Manager – provides common services and allocates resources to all tasks operating under System 700.
- Clock Manager – performs three types of time sequencing functions for program execution:
  - Absolute Time Sequencing: where programs are exexuted on an absolute time-of-day basis.
  - Elapsed Time Scheduling: where the user may specify periodic execution of a program on an elapsed time interval basis.
  - Program Suspension: where program execution is suspended for a specified time interval, with the Executive returning control to the program after the time interval elapses.
- Memory Manager – allocates core and disk storage to various programs.
  - Overlay Core: allows several different programs to share the same memory space.
  - Free Core Allocation: satisfies program and buffer requests for memory space and retrieves memory space after the program is completed.
- Queue Manager – arranges and modifies the various FIFO (First-In/First-Out) queues required by the Executive.
- Device coordination (lockout) – used to reserve a particular device in a multiprogramming environment.
- Re-entrancy of user programs – allows several different users to use the same program simultaneously.
- Input/Output Manager – provides centralized control of the I/O devices.
- Error Processor – provides centralized processing of run-time errors.
- Interrupt Processor – provides centralized processing of all interrupt requests.

OS/700 Subsystems

The various subsystems that will be available with OS/700 include the following:

- Fortran IV Compiler – a general-purpose, higher level programming language resembling the symbolic language of mathematics. The user can write all his programs in Fortran, including real-time input/output response and time sequencing.
- DAP/700 Macro Assembler – which enables symbolic programming while maintaining the characteristics, flexibility, speed, and precision of machine language programming. This assembler supports the use of a separate macro definintion library as well as macro definitions in the program.
- BASIC Interpreter – a stand-alone language processor that provides an interactive environment in which a user can compose, edit, and execute programs written in the BASIC language. The user can assemble an entire program and call for its execution, or he can enter statements to be executed immediately.
- Linkage Editor – links the object text output of the assembler to form a core image for loading directly into memory.
- Configurator – provides a system generation capability to simplify the process of configuring a user's system.
- Utility Routines – an expanding set of utility routines; include the following:
  - Source Update: for updating and correcting user programs.
  - Debug: an interactive run-time capability for analyzing execution errors.
  - Transfer and Verify: for transferring programs or data from one storage medium to another, as well as verifying the accuracy of the copy.

OS/700 Module Libraries

The OS/700 Module Libraries are designed to satisfy the need for functional routines in support of special applications. With these modules the effort to generate a special-purpose system is significantly reduced. The Module Libraries will consist of the following:

- Communication Modules – These modules provide the user with the ability to support a variety of terminal devices via a multiline controller and communicate with a host via a single-line controller.
  - Terminal Control Processor: supports various modules allowing different types of input and output, various timing requirements, a variety of data structures, and different line types.

- Host Control Processor: requests bids for obtaining master status, prepares transmission units for output to the host, interrupts answer backs to bids and transmission units.

- Sensor-Based Modules – These modules allow the user to communicate with the following I/O systems:
  - Analog Input: includes automatic correction for errors.
  - Digital Input: supports the status input modules of the Real-Time Interface (RTI).
  - Asynchronous Input: supports the broad areas of sensors for digital tracking and terminal data entry systems.
  - Counters: supports event and preset counters.
  - Digital Output: allows the user to address various types of digital output.
- Executive Modules – These are the components of the OS/700 Executive. By selecting only those components which are required for the specific application, the user can reduce his configuration requirements to a minimum. It is easy for each user to generate a system tailored to his specific needs.

Equipment Requirements

The minimum hardware requirements for OS/700 are as follows:

- A Type 716 Central Processor with 16K words (32 K bytes) of main memory.
- One disk device with a minimum of 128K words of storage.
- A program input/output device.

LANGUAGE PROCESSORS

System 700 will be supported by a choice of languages: the DAP/700 Macro Assembler, a BASIC Interpreter, a Linkage Editor, and ANSI Fortran IV.

DAP/700 Macro Assembler

DAP/700 will provide a symbolic programming language while maintaining the characteristics, flexibility, speed, and precision of machine language. Operating as a subsystem under OS/700, it will provide numerous pseudo-operations which offer convenient programmer-defined assembly and linkage controls, data definitions, and program linkages.

DAP/700 will allow the programmer to define and use macro instructions. This is advantageous whenever a program contains a repeated, parameterized pattern. Several statements are then replaced by one, and the pattern in varied by changing the parameters. This is especially beneficial for establishing system-level and installation-wide software interfaces or calls. To facilitate this objective, DAP/700 can accept a macro library as a separate input.

Honeywell will provide a compatible macro assembler as part of the Host-Resident Software System.

DAP/700 PROGRAMMING

When a program is written in the DAP/700 Macro Assembly Language, the code is prepared first and then corrected by use of the source update program. If the program uses macros, the macro definitions can be obtained from three sources (see Figure 12); these may appear in the program itself, in a separate macro library, or from OS/700, in the case of a predefined OS/700 macro.

The DAP/700 assembler will generate an object program (for subsequent linking) and an expanded listing. The listing contains the source code, the octal equivalent generated by the assembler, error flags for all syntactic errors, and an alphabetic list of the symbols used. Even when errors are detected, the assembler usually produces an object program usable by the programmer. If necessary, the program is corrected and the process repeated until the programmer decides to run the object text. Then the object program is linked, a memory map is obtained, the link text is loaded, and execution begins.

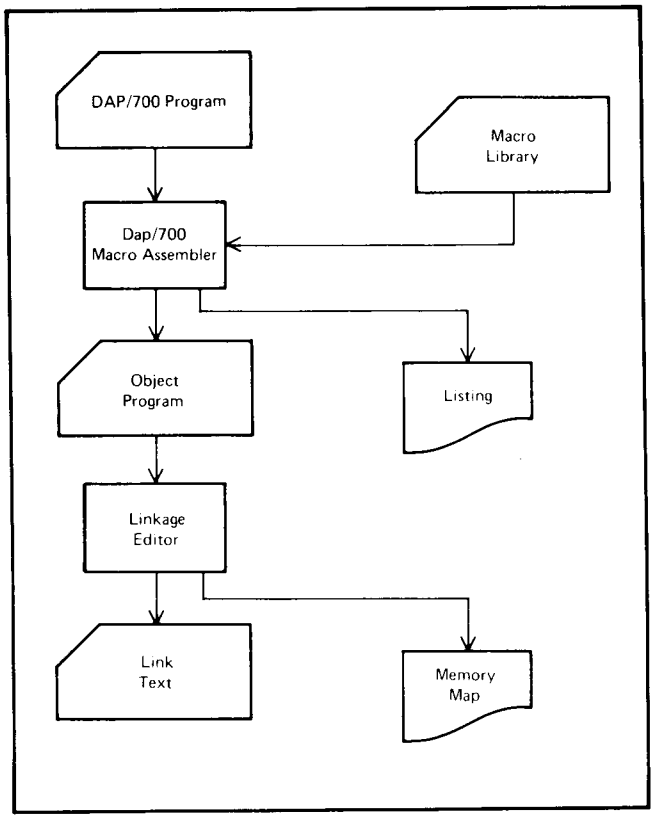


Figure 12. DAP/700 Programming

FEATURES

Desectoring

Without indirect addressing or indexing, only 1,024 locations are directly addressable from a given location. To access elsewhere, indirect addressing or indexing is required. The assembler and linkage editor allow the programmer to ignore this task, called desectoring, by taking care of it for him. Alternatively, the programmer can specify all or part of the desectoring and leave the rest to the software.

Subroutine Linkages

Through the CALL pseudo-operation, DAP/700 provides linkages to external subroutines. The calling sequences are compatible with Fortran IV, so that all library facilities support the two languages.

Expressions and Literals

Compound expressions and several types of literals facilitate programming. Compound expressions consist of one or more operands separated by arithmetic operations. Literals consist of decimal, octal, hexadecimal, and ANSI alphanumerics.

Fortran-compatible common storage allocation features assign cells in memory to interprogram communication, providing a Fortran-like common storage facility. The contents of these cells can be preset with a capability analogous to that of the Fortran DATA statements.

Symbol Definition

Three pseudo-operations allow a symbol to be assigned either absolute or relocatable values. The symbols may then be referenced in other assembly language statements. One of these pseudo-operations is used for redefining symbols.

External Addressing

A pseudo-operation enables the user to declare a symbol as being in an external subprogram. When the symbol is encountered in the address field of a memory reference instruction, the necessary linkage information is generated so the address can be completed by the linkage editor. Device addresses for input/output instructions may be external symbols.

Control of Assembly Process

The user can choose the assembly of absolute or relocatable code and can invoke or suppress the desectoring mode.

Conditional Assembly

Condition-testing pseudo-operations enable the user to test an expression's value. Depending on the outcome of this test, the assembler suspends or continues code generation until either the assembly-mode switching pseudo-operation or the end-of-range pseudo-operation is encountered. The mode-switching pseudo-operation reverses the assembly mode. It is effective only within the range of the condition-testing pseudo-operation.

Other features of DAP/700 will include:

- Free field format
- Literal operands

BASIC Interpreter

The System 700 BASIC Interpreter will provide an interactive environment in which a user can compose, edit, debug, and execute programs written in the BASIC language. The user can store an entire program and call for its execution, or have the statements executed immediately.

SPECIAL FEATURES

- Superset of Dartmouth BASIC
- Multiple statements per line
- Immediate statement execution, interactive programming
- System level commands
- Multidimensional arrays
- Unrestricted subscript expressions
- CALL to DAP/700 and Fortran subroutines

ADVANTAGES

- Many years of use
- Useful for general problem solving
- Easy to learn, easy to use
- Fast debugging

INITIALIZING PROCEDURES

When BASIC is loaded, the user has the option of enlarging other program storage areas by aborting the trigonometric functions. After loading and initialization, input is requested by a question mark. The programmer responds with either a statement in the BASIC language or a command to the Interpreter

MODES OF EXECUTION

Statements may be stored in memory for later execution, or punched on paper tape, or executed immediately in an interactive manner as though they are commands.

The absence of a line number informs the Interpreter that immediate execution is required. DATA, DIMENSION, and DEFINE statements cannot be executed in the immediate mode.

The two modes of execution can be used to complement one another. When a stored program stops executing because an error has been detected, immediate statements

can be used to PRINT the current value of variables or to start another program. As an alternative, the values of variables can be initialized or changed and the program restarted where execution stopped.

STATEMENT EDITING AND REFERENCING

A line can be deleted by typing its number followed by a carriage return. When inputting a statement, the last character typed can be removed by typing a backward arrow (←). A commercial at symbol (@) deletes the line. More than one statement may be placed on a line by separating the statements with colons.

When an immediate statement (e.g., GO TO) refers to a line number, the line is assumed to be in the stored program. Hence, GO TO will cause the stored program to begin executing at the specified line.

CALL STATEMENT

To interface with a subroutine written in Fortran or DAP/700, the subroutine is loaded in an area of upper memory not used by BASIC. When the programmer initializes the Interpreter, he specifies the highest location in memory usable by BASIC (a location below his subroutines). The entry points to the subroutines are entered in a table, whose address is contained in location 776. Location 777 contains a pointer to the first cell in the base sector which can be used for desectoring.

Up to 10 subroutines may be loaded. They are called as follows:

CALL (<Subroutine Number>, <Argument List>)

BASIC PROGRAMMING EXAMPLES

The following four programs were written to solve the equation

$$X^2 + 2X - 4 = 0$$

for one of the two roots. The formula for the roots is

$$\frac{-B \pm \sqrt{B^2 - 4AC}}{2A}$$

and A = 1, B = 2, and C = –4. The computer supplied the underscored responses:

a. Use of READ and DATA Statements for Variables

```
? JOB
? 10 READ A,B,C
?20 LET X = (-B + (B ↑ 2-4*A*C) ↑ 0.5)/(2*A)
?30 DATA 1,2 - ←, -4
?40 PRINT "ROOT IS", X
?50 END
?RUN
ROOT IS          1.23607
50 EXIT
?
```

b. Use of Data Constants

```
?JOB
?10 LET X = (-2 + (2 ↑ 2-4* 1* (-4)) ↑ 0.5/(2* 1)
?20 PRINT "ROOT IS", X@
?20 PRINT "ROOT IS", X
?30 END
?RUN
ROOT IS          1.23607
30 EXIT
?
```

c. Use of INPUT Statement

```
?JOB
?10 INPUT A,B,C
?20 LET X = (-B + (B ↑ 2.4* A* C) ↑ 0.5)/(2* A)
?40 PRINT "ROOT IS", X
?50 END
?RUN
!1,2,-4
ROOT IS          1.23607
50 EXIT
?
```

d. Use of Arithmetic Calculator Loop

```
?JOB
?10 INPUT 1: PRINT 1: GO TO 10
?RUN
!(-2 + (2 ↑ 2-4* 1* ( -4)) ↑ 0.5)/(2* 1)
1.23607
?
```

LANGUAGE SUMMARY

A BASIC program consists of a set of statements terminated by an END statement. Each statement in a stored program must be numbered. Unnumbered statements are executed immediately. Table 8 lists the major constituents of the BASIC language. The angular and square brackets in the table represent variables and optional elements, respectively.

The LET and GO TO are the assignment and control transfer statements, respectively. The GO SUB is a subroutine call. Functions are invoked by enclosing the parameter in parentheses following the function name. The IF . . . THEN allows a single relational operator between expressions, and control passes to the statement number following the THEN if the relation is true. NEXT is used to terminate the range of the FOR statement and must use exactly the

same variable as in the FOR statement. If the third expression in a FOR statement is omitted, it is assumed to be one. The expression in the ON statement is evaluated and truncated to an integer. For expression = 1, control is transferred to the first statement number in the list; for expression = 2, control is transferred to the second statement number in the list, etc.

TABLE 8. BASIC LANGUAGE SUMMARY

```
CALL (<subroutines number>, <argument list>)
DATA<number>, <number>, . . . , <number>
DEF FN<letter>(<unsubscripted variable>) = <expression>
DIM<variable>(<integer>[,<integer>] . . . )
END
FOR<unsubscripted variable> = <expression>TO<expression>STEP<expression>
GO SUB<statement number>
GO TO<statement number>
IF<expression><relation><expression>THEN<statement number>
INPUT<variable>,<variable>, . . . ,<variable>
[LET] <variable>[<variable>] . . . =<expression>
NEXT<unsubscripted variable>
ON<expression>GO TO<statement number>[,<statement number>] . . .
PRINT<literal or expression>,<literal or expression>, . . .
READ<variable>,<variable>, . . . ,<variable>
REM<any string of characters>
RESTORE
RETURN
STOP
```

TABLE 9. BASIC COMMANDS

JOB	Clears the program and data values area in memory
CLEAR	Clears the data values array in memory
PUNCH	Punches a paper tape on the teletypewriter or paper tape punch
LOAD	Loads a paper tape on the teletypewriter or paper tape reader
RUN	Begins to execute the program at its first statement; a CLEAR command is assumed
RUN<statement number>	Begins to execute the program at the statement specified
LIST	Lists the program on the teletypewriter
LIST<statement number>	Lists the program starting at the statement specified
LIST<statement number>,<statement number>	Lists the statements between the given numbers
CONTINUE	Continues execution where it stopped after sense switch 1 was set[1]
QUIT	The computer HALTs

[1] When sense switch 1 is set, BASIC types the line number being executed followed by "BREAK", and returns to the command mode.

The READ assigns to the listed variables the values obtained from a DATA statement. The latter is used to specify all the values needed for the variables. For output, the user can specify variable names or literals; the literals are enclosed within quotation marks. Thus, if X is 625, the statement PRINT "THE SQUARE ROOT OF" X, "IS" SQR(X) causes the following to be printed: THE SQUARE ROOT OF 625 IS 25. For normal printing purposes, the output line is divided into five zones of 13 spaces each. The user can change the width of these zones, however, through the use of commas and semicolons. a PRINT statement without anything following it signals a new line.

The program terminates with the END statement; the STOP returns BASIC to the command mode.

The CALL statement is used to invoke one of up to 10 subroutines written in Fortran IV and the DAP/700 Macro Assembly Language. The entry points of the subroutines are inserted into a table maintained by the Interpreter. The subroutine number tells BASIC which table entry to use.

The DIMENSION statement is used for subscripts whose value exceeds 10. DATA specifies the input constants. RESTORE returns the DATA pointer to the first constant of the first DATA statement. An INPUT statement types an exclamation point and the program waits for the user to type in the data items requested in the READ list.

Functions are defined by the DEF statement; the function name consists of the letters FN followed by a letter. Any expression which fits on one line can be used to define a function, including another function.

REM statements are nonexecutable and are used to enter comments and explanations in the program listing.

CONFIGURATIONS

Required Hardware

- System 700 computer
- 4K-word main memory
- ASR-33 or -35 teletypewriter

Supported Hardware

- High-speed paper tape reader/punch
- 16K-word memory

TABLE 10. BUILT-IN BASIC FUNCTIONS

Function Reference	Mathematical Equivalent
ABS(X)	$\|x\|$ The absolute value of magnitude of the argument x
ATN(X)	$\tan^{-1}$ (x) The arctangent in radians of the argument x
COS(X)	cos(x) The trigonometric cosine of the argument x, where x is in radians
EXP(X)	e^x The exponential function
INT(X)	The largest integer less than or equal to the argument x; only magnitude is considered INT (+ 1.5) = 1 INT (- 1.5) = 1
LOG(X)	$\log_e$ (x) The logarithm to the base e of the argument
RND(X)	Random number generator; the first time the function is used, the argument should be nonzero to initialize the generator; subsequent calls to generate random numbers should be made with the argument equal to zero
SGN(X)	The sign of the argument x x<0, SGN (x) = -1 x = 0, SGN (x) = 0 x>0, SGN (x) = 1
SQR(X)	$\sqrt{x}$, $x \geq 0$ The positive square root of the argument; the argument must be greater than or equal to zero
SIN(X)	sin(x) The trigonometric sine of the argument x, where x is in radians
TAN(X)	tan(x) The tangent of the argument x, assuming x is in radians

TABLE 11. BASIC DIAGNOSTICS

AS	Array subscript out of bounds
DA	Attempt to READ more data than available
DF	Attempt to use a function deletion during initialization
DL	Statement terminator error
DP	Two decimal points in a number
DV	Dummy variable in DEF statement is subscripted
DZ	Divide by zero
FD	Invalid delimiter in FOR statement
FN	Characters FN misplaced in DEF statement
GS	GO SUBs nested more than eight deep
IC	Condition in IF statement is incorrect
ID	General error
IV	Index variable in FOR statement is subscripted
LG	Negative logarithmic function argument
MO	Memory overflow
M,	Missing of misplaced comma
M=	Missing or misplaced equals sign
M)	Missing or misplaced right parenthesis
M(	Missing or misplaced left parenthesis
NO	Numerical overflow
NU	Numerical underflow
NX	Next statement has no matching FOR
ON	Expression in ON statement is nonpositive, as the GO TO is missing
PD	Strange item delimiter in PRINT statement
RT	RETURN statement not in subroutine
SN	Statement number error (range 1 to 9999)
SQ	Negative square root function argument
SS	Subroutine selector in CALL out of range (1 to 10) or subroutine is missing
TH	THEN left out of IF statement
TX	No end of quote
UF	Undefined function
UM	Unary minus error
US	Undefined statement number
UV	Undefined variable

Linkage Editor

The Linkage Editor is a single-pass program which accepts object modules produced by the assembler and links them together to produce a link text of the combined program with external references resolved (see Figure 13). The resulting link text, which is essentially an absolute memory image of the program, is loaded by the link text loaders. The Linkage Editor supports all the assembler features, allows for program identification in the resultant link text, address control, the saving to system addresses for later partial loads, memory maps, and free space utilization.

Link text loaders are provided for paper tape, punched cards, and 7-track magnetic tape. Using the appropriate key-in loader, the loaders will load link text into System 700, print the identification of the program being loaded, load the program, and start execution at the specified address in the link text.

The Linkage Editor will be provided as a subsystem of OS/700 and runs under its Executive. Honeywell will provide a compatible Linkage Editor as part of the Host-Resident Software System.

FEATURES

- Maximum space for user programs, because minimum space is required for loading.
- Error message reporting of linking problems to the user. The error messages include the following:
  - CE – Command error; the rest of the command line is ignored and another command is solicited.
  - RS – Object text record sequence error.
  - BL – Object text block type error.
  - TI – Illegal object text type; this should never occur.
  - TO – Symbol table overflow.
  - BO – Primary base areas overflow.
- Conversational control of linking and full reporting of information via the teletypewriter.
- Extensive control of linking and desectoring to provide optional use of core memory and complete user flexibility.

OPERATING OVERVIEW

Once the object text modules have been prepared, the program is ready for linking and loading. The programmer supplies control information to direct the Linkage Editor via the Command Input stream. The object text modules are then read and combined into a link text module ready for loading with all external references resolved. A memory map is also produced by the Linkage Editor, to aid in program debugging. The link text version of the program is then loaded and run-time debugging begins.

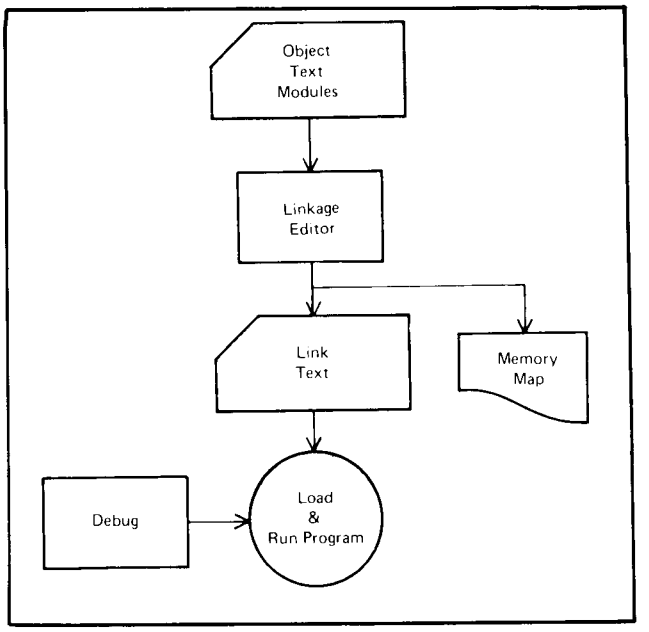


Figure 13. Linkage Editing

MAJOR COMMANDS

- Address command – lets user establish the starting address.
- Base command – lets user establish the base sector for desectoring.
- BSD command – establishes the area for desectoring outside the base sector.
- Symbol Definition command – allows the user to define external symbols at linking time.
- Force command – allows the user to force link modules.
- Total command – allows the user to force-link an entire library.
- Library command – tells OS/700 to satisfy external references from the OS/700 module library.
- Identification command – lets the user establish his identification, which subsequently identifies the program at run time.
- Symbol Table command – saves the symbol table, to allow partial loading.
- Link command – starts the Linkage Editor.
- Define command – allows the user to define external symbols at linkage time.

Fortran IV

Fortran IV is a general-purpose, higher level programming language closely resembling the symbolic language of mathematics. It is procedure-oriented, problem-oriented, problem-solving. For a problem involving a large number of variables, the scientist, engineer, or programmer is provided a clear, precise method of expressing his problem and arriving at the solution.

The Fortran subsystem will perform input/output through OS/700 Input/Output Supervisor. It will be supported by drivers, a run-time I/O library, and a mathematical subroutine library. It conforms to ANSI Fortran standards and is substantially the same Fortran language as that available on all large computers. Thus it can draw on an extensive reservoir of existing routines.

Fortran IV will be provided as a subsystem of OS/700 and will run under its executive.

ADVANTAGES OF FORTRAN

- Because Fortran uses terms already familiar to the scientist, engineer, or mathematician, it is easy to learn and to use.
- The use of procedure-oriented terms and statements eliminates the need for detail coding and reduces the chance of coding errors.
- Fortran uses one statement to replace many assembly language instructions; this reduces the time and cost normally associated with programming.
- Fortran IV programs are virtually self-documenting; this permits the work of one user to be referenced, maintained, or altered by another with ease.
- Program correction is simplified because error diagnostics are automatically inserted with the object program listing by the compiler.
- If necessary, large Fortran IV programs can be segmented into smaller, more manageable amounts of coding.
- Assembly language routines and subroutines, including any mathematic routines in the OS/700 library, can be inserted in a Fortran IV program.

FEATURES OF OS/700 FORTRAN

- ANSI Fortran IV compatibility: all the advantages of a standardized language.
- Run-Time Trace Capability: faster and more accurate debugging. Three kinds of trace capabilities are available:
  - Symbolic trace, which allows the programmer to specify symbols, with values produced as output every time they are changed.
  - Area Trace, which results in outputting every value as it is computed in a specified sequence of statements. In this way, unusual values can be spotted quickly.
  - Label Trace, which outputs statement numbers only.
- Program-Chaining: an overlay capability to accommodate programs too large for the main memory of the computer. Allows the programmer to segment his program in such a way that only one segment is core-resident at any one time.
- Mixed-mode arithmetic.
- Octal constants, hexidecimal constants.
- Optional compilation of selected statements.
- Quoted Hollerith strings.
- Memory-to-memory format conversions.
- Conditional Compilation: Selective compilation of program statements; i.e., all statements in which 'X', 'Y', 'Z', or 'W' appears in column 1 can be treated selectively as remarks or as executable statements as specified in the Fortran job command.
- In-line assembly language code.
- Real-time statements to give the Fortran programmer access to the full capabilities of the OS/700 Executive.

FORTRAN PROGRAMMING

To use the Fortran compiler, the programmer first prepares a source program on one of several recording media, e.g., cards. The compiler then reads the program in a single pass over the source cards and produces DAP/700 assembly language translation plus a program listing. The DAP/700 code is then assembled to produce object text.

Honeywell's Fortran IV subsystem provides compilation-time debugging aids. If there are syntactic errors, each is indicated on the listing following the statement in which it occurs. In this way, the errors are most easily located and corrected. The program is recompiled until there are no syntactic errors. Now the program is run and tested to complete the debugging process.

TEST AND MAINTENANCE ROUTINES

Honeywell Test and Maintenance (T and M) Routines identify problem areas, localize incorrect operation, and verify correct operation of the central processor, its associated features, and peripheral devices. The routines simulate actual operation so as to establish levels of performance and facilitate normal preventive maintenance. They exercise recognized potential failure modes and furnish specific evidence of error-free operation.

These routines apply to the entire range of available options, and they do not require an operating system. All are normally supplied in a self-loading format to minimize the loading effort and core requirements.

Program Characteristics

T and M routines test circuit logic, device functions, and equipment performance levels.

Programs verify the correct operation of logic circuits by isolating and exercising the logic functions they perform.

During logic testing, operator intervention is minimized, if required at all.

Tests on I/O devices require that all control functions and data paths be operational. Wherever possible, closed-loop tests are performed to verify correct operation automatically. Device tests identify failing control functions to the maintenance engineer and indicate failing data by bit position. Many I/O device controllers have test modes. These are used to force or simulate error conditions and to facilitate the localizing of actual failures.

All tests operate for a specific time period to establish a level of equipment performance. Tests for devices requiring periodic adjustment contain supporting sections so that adjustments may be accomplished easily.

Mainframe Programs

CENTRAL PROCESSOR ROUTINE: AB16-CCT4
Tests all standard central processor features, instructions, and address generation. Dynamically relocates itself throughout memory.

MEMORY ROUTINE: AB16-CMT4
Determines the type and size of memory and tests the memory system. Specifically considers power supply sensitivity, worstcase pattern, random data and timing, and bit-cell addressing uniqueness.

POWER FAILURE INTERRUPT/RESTART ROUTINE: AE16-PFT3
Ensures that a power failure does not disturb memory contents and that the proper action (interrupt or restart) is taken. If the interrupt mode is selected, the program exercises the processor and random memory locations for one millisecond before halting.

EXTENDED ADDRESSING ROUTINE: AB16-05T2
Tests the extended address formation logic whether extended memory is present or not.

MEMORY PARITY ROUTINE: AE16-07T2
Tests the parity generation logic. Requires that a jumper wire be added, since the logic is not normally under program control. AB16-CMT4 (Memory) and AE16-PFT3 (Power Failure Interrupt/Restart) ensure that parity indications do not occur unexpectedly.

MEMORY LOCKOUT AND BASE SECTOR RELOCATION ROUTINE: AE16-08T2
Tests features of the Memory Lockout option and/or the Base Sector Relocation option.

HIGH-SPEED ARITHMETIC ROUTINE: AB16-11T1
Tests the added features of this option, which include the MPY (multiply) and DIV (divide) instructions and the double-register operations.

REAL-TIME CLOCK ROUTINE: AB16-12T3
Tests short-term (single-period) and long-term (several seconds) stability. Indicates local accuracy with respect to the central processor clock and global accuracy with respect to operator-observed real time.

REAL-TIME CLOCK/WATCHDOG TIMER ROUTINE: AA16-3000T1
Tests as above for both the line-driven and crystal-driven clocks. The Watchdog Timer is tested for correct time and the ability to break into halts and infinite indirect-address loops.

Device Programs

TELETYPEWRITER ROUTINE: AG16-TWT1
Tests the keyboard, page printer, tape reader, and tape punch for correct operation.

PAPER TAPE READER AND PAPER TAPE PUNCH ROUTINE: AG16-RPT2
Tests the reader and punch as a combination or the reader alone via a prepunched test tape. Exercises with random data and timing.

CARD READER ROUTINE: AB16-CRT3
Tests the 800-cpm reader in both Hollerith and binary modes. Hollerith and binary modes. Hollerith is tested by reading a prepunched deck. Binary is tested by repeated passes through a user-supplied random deck limited only by the size of the memory (seven words per card).

CARD READER/PUNCH ROUTINE: AB16-RPT3
Tests the reader portion exactly as the 800-cpm reader is tested. Tests the punch portion by punching a 1000-card set of random numbers, using random timing, and then reading the deck.

LINE PRINTER ROUTINE: AB16-55T3
Tests the 300-lpm printer for all features.

MAGNETIC TAPE UNIT ROUTINES
(7 TRACK): AE 16-MTT2
(9 TRACK): AA16-4170T1
Tests the tape system in all modes, using fixed and random data and timing for both read and write. Reads previously prepared tapes or prepares them during the test. Uses all

of available memory. Up to four 9-track drives may be exercised simultaneously.

REMOVABLE DISK SUBSYSTEM ROUTINE: AB16-47T3

Tests the 10- or 20-surface mass-storage system for formatting, reading, writing, multiple unit seeking, and simultaneous data transfer. Uses random data and parameters. Can read previously written packs or write on compatible packs. Permits selected portions of the pack in use to be tested individually; also includes a total-pack test feature. Uses all of available memory.

FIXED-HEAD DISK SUBSYSTEM ROUTINE: AA16-4511T1

Tests the mass-storage system for reading, writing, lockout protection, and access time. All of available memory is used. The program uses random data, track and sector selection, length of transfer, and time to test the area specified by the operator.

HOST-RESIDENT SOFTWARE SYSTEM

Honeywell's Host-Resident Software (HRS) system will allow a user to develop System 700 software programs on a host computer where a larger memory and a variety of data processing peripherals are available to do the job. After assembly, the new programs can be transmitted down-line to the remote System 700 computer. The HRS system will enable a user to keep his System 700 costs to a minimum without sacrificing software development flexibility. The Host-Resident Software System is completely coded in ANSI standard Fortran IV. This is substantially the same Fortran language as that available on all large computers.

If a Fortran compiler is available on the host system, HRS is a convenient alternative programming tool, whether or not the System 700 is located remotely.

Some of the outstanding features of HRS are as follows:

- Convenient program development.
- A computer-independent software system.
- Minimized remote-hardware costs.
- The flexibility of a large computer system for program development.
- Use of down-line loading.

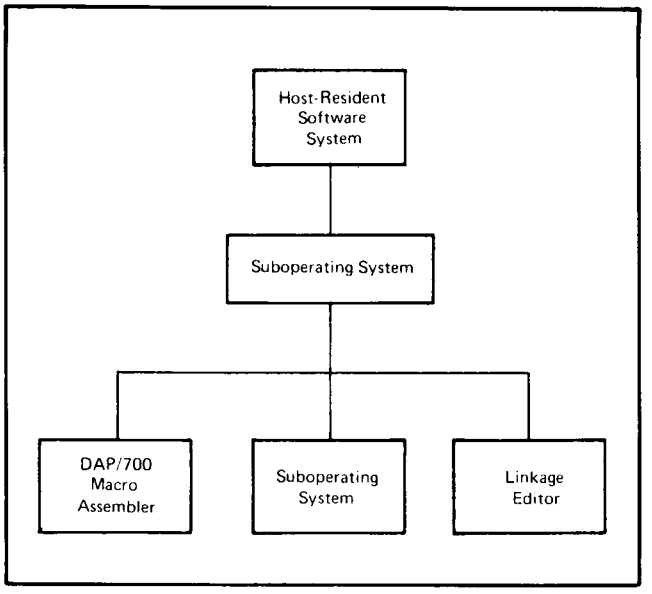


Figure 14. Host-Resident Software System

- Complete coding in ANSI Fortran IV.
- Ease of conversion to another host computer, because Fortran is the implementation language.

HRS will consist of the DAP/700 Macro Assembler, Linkage Editor, and Configurator, and a Suboperating System (see Figure 14). The Suboperating System provides centralized control and a standard interface between the other components of HRS and various host computer file systems and JCL structures. The Suboperating System is machine-dependent: Honeywell provides it for Series 200 and 2000.

The DAP/700 Macro Assembler and the Linkage Editor offer the same capabilities as their counterparts under OS/700. A user can code assembly language programs and produce object and link text on either a System 700 or a host computer. Operating as a component of HRS, the DAP/700 Macro Assembler provides numerous pseudo-operations which offer convenient programmer-defined assembly and linking controls, data definitions, and program linkages.

The HRS Configurator will operate in conjunction with the DAP/700 Macro Assembler and Linkage Editor and the Suboperating System to perform the task of system generation. With the Configurator, a specific configuration can easily be generated to support a user's particular application requirements and hardware environment.

```
37    000004       Q4     OCT   4                    NEVER
40    0 01 00055          JMP   SRT5                 END O
41    0 01 00026          JMP   SRT1                 MORE
                     *
42    0 04 00373 SRT3     STA   PIC2                 PIC2
43    0 10 00204          JST   LCHK
44    0 01 00050          JMP   SRT2
45    0 10 00127          JST   GRIT                 FETCH
46    101040              SNZ                        SKIP
47    0 01 00105          JMP   SWAP                 INTER
50    0 02 00373 SRT2     LDA   PIC2                 TRY N
51    0 07 00377          SUB   Q3
52    0 11 00372          CAS   PIC1                 TEST
53    0 01 00042          JMP   SRT3                 NO -
54    0 04 00373          STA   PIC2                 YES -
55    0 02 00373 SRT5     LDA   PIC2                 DROP
56    1 04 00000          STA   T237,1
57    1 13 00000          IMA   T136,1
60    1 04 00000          STA   T137,1
61    0 12 00000          IRS   0                    INCRE
62    0 01 00017          JMP   SRT7                 GO SO
63    0 02 00402          LDA   MQ1                  SEARC
64    100000              SKP
65    0 02 00000 SRT6     LDA   0                    DECRE
66    0 07 00401          SUB   Q1
67    0 04 00000          STA   0                    REPLA
70    0 07 00376          SUB   M36                  TEST
71    100400              SPL                        SKIP
72    0 01 00216          JMP   DUMP                 SORT
73    1 02 00000          LDA   T136,1                FETCH
74    100400              SPL                        SKIP
75    0 01 00065          JMP   SRT6                 SORTE
76    1 04 00000          STA   T137,1               SET
77    140500              SSM                        MARK
00    1 04 00000          STA   T136,1               AND D
01    1 02 00000          LDA   T236,1
02    1 04 00000          STA   T237,1
03    0 12 00000          IRS   0                    SET E
04    0 01 00017          JMP   SRT7                 GO SO
                     *
05    0 02 00372 SWAP     LDA   PIC1                 HERE
06    141206              AOA
```

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